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DESIGN AND DEVELOPMENT OF AN AUTOMATED DEMODULATOR CALIBRATION STATION

by

Eng, Chun Heong

December 2009

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13. ABSTRACT (maximum 200 words)

This thesis describes the design and development of an automated demodulator calibration station. Many commercial demodulator boards have an inherent problem of DC offset due to their direct down conversion architecture. It is necessary to measure the DC offset and compensate for it when the demodulator is used in a system such as a digital phase array.

The proposed automated calibration station uses a combination of COTS hardware and software, such as NI PXI-1044 (PC) and LabVIEW programs, to digitally generate I and Q signals. The LabVIEW program cycles through phase shifts over a range of 0^0 to 360^0. These signals are converted into analog outputs using NI PXI-6704 (DAC). Subsequently, these converted analog signals are fed into the modulator, going through an upconversion modulation process with an RF output. This RF output is adjusted to meet RFIN specification of the quadrature demodulator board before feeding into the board to recover the I and Q control signals, which are sampled by the NI PXI-5112 digitizer. After the full cycling of phase shifting by the modulator is completed, I and Q offsets are computed.

This station has improvements over the existing manual calibration station, such as ease of use, shorter calibration time, accuracy and versatility for future modifications and improvements.

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DESIGN AND DEVELOPMENT OF AN AUTOMATED DEMODULATOR CALIBRATION STATION

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EXECUTIVE SUMMARY

With rapid technological advancement in our present modern era, commercial and military wireless communications applications have inevitably become part of our daily activities. Most modern systems use quadrature demodulation, where the receiver has two channels: in phase (I) and quadrature (Q). However, some design issues arise due to certain inherent characteristics of the direct conversion architecture used in many receivers. They include DC offset errors, I and Q mismatch, and even order harmonic distortion. These errors cause problems when the demodulators are used in systems. Consequently calibration of a direct conversion demodulator board is required in order to calculate the offset errors and compensate for the phase errors during beam-forming and demodulation processing.

This thesis carried out the design and development of a AD8347 demodulator automated calibration station. It improves the existing manual calibration station on parameters such as ease of use, decreasing the duration of the overall calibration process, improving the accuracy of the post calibration DC offset results by using averaging of multiple tests on a single demodulator board, and versatility for future modifications and bread-boarding.

Several validation tests were conducted to verify the hardware and software of this new automated calibration station. The test conducted to validate the automated station against the manual calibration gave I and Q offset values that were almost the same with only less than 3.15 % difference. It is believed that the automated test is actually more accurate, because the mechanical phase shifter introduced error due to wear and tear, dirt, etc.

The automated calibration process was also more time efficient, taking only 1/10 of the manual calibration duration and helping the user avoid the chore of manually turning the phase shifters. Tests were carried out to characterize the performance of the new automated calibration station.

Six AD8347 demodulator cards used in the tracking array developed for UAV Digital Tracking Array were calibrated using the station described in this thesis to further explore its operational aspect. With calibrated I and Q offset values, the tracking array is able to retrieve the phase information of the incoming waveform thereby allowing the array to successfully track an incoming signal. Thus, the test indicates a successful implementation of the AD8347 demodulator card using this new automated calibration station.

LIST OF ACRONYMS AND ABBREVIATIONS

ADC	analog-to-digital convertor
AGC	automatic gain control
AOA	angle of arrival
BAMP	baseband differential instrumentation amplifier
BIT	built in test
DAC	digital-to-analog convertor
DC or dc	direct current (zero frequency)
DDAR	distributed digital array radar
DF	direction finding
DUT	device under test
FOV	field of view
GUI	graphical user interface
IF	intermediate frequency
I	in phase
IC	integrated circuit
LNA	low noise amplifier
LPF	low pass filter
LO	local oscillator
LOS	line-of-sight
NI	National Instruments
NPS	Naval Postgraduate School
PC	personal computer
PCI	peripheral component interconnect
RF	radio frequency
RFI	radio frequency interference
RSNS	robust symmetrical number system
RX	receive
Q	quadrature
TX	transmit
VGA	variable gain amplifier

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I. INTRODUCTION

A. BACKGROUND

With rapid technological advancement in our present modern era, wireless communications has inevitably become part of our daily activities. The technology has been applied to a wide range of commercial and military applications such as TV broadcast, mobile phone, wireless internet, radar and electronic warfare.

There are several stages of signal processing in a modern digital transmission and reception system as shown in Figure 1. They include the transmitter section on the left, the radio frequency (RF) propagation channel at center and the receiver section on the right side.

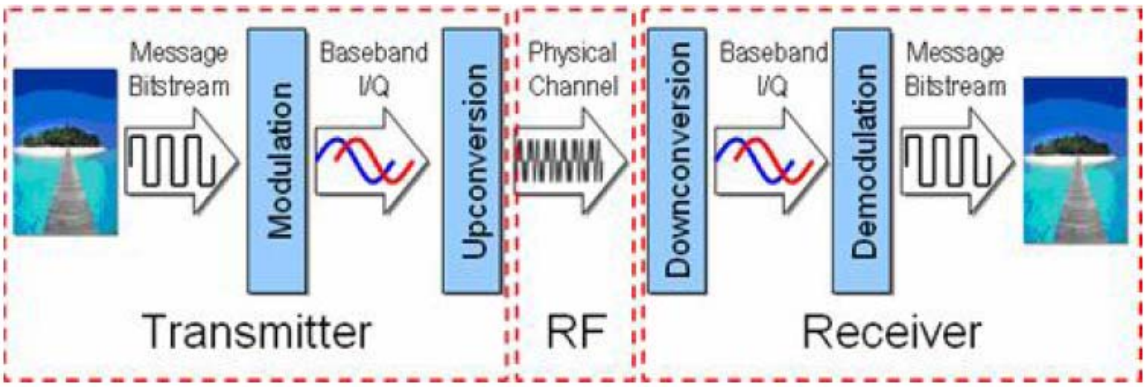

Figure 1. Communication Block Diagram (From: [1]).

The first stage is the transmission process, which starts with the modulation of a message or data onto a RF signal. The upconverted signal is broadcast over the channel, either hard wired or wireless, then down converted and demodulated for extraction of the intended message at the receiver.

There are several receiver architectures, such as the heterodyne system, superheterodyne system, and direct conversion (homodyne) system, being commonly used in many wireless devices. Both heterodyne and superheterodyne are commonly used technologies that employ two stages of detection and filtering first to translate the signal from the carrier frequency to an intermediate frequency (IF) before proceeding on to the

final stage of modulation to baseband. These systems require additional IF circuitry making them bulkier than direct conversion systems. Because of this particular advantage of using fewer components, the direct conversion transmitter and receiver are comparably smaller in size. This is one of the reasons why this communication method has overtaken other methods to become popular with most wireless device designers.

Direct conversion architecture was developed in 1932 to improve on the superheterdyne method. However, direct conversion did not enjoy much popularity initially, until the development of integrated circuitry. Practical implementation requires an additional phase-lock-loop circuitry with tight tolerance components; thus implementing it without integrated circuitry (IC) makes it expensive. With integrated circuit technology, low tolerance phase-locked-loop components can be integrated into low cost IC packages.

Most modern systems use quadrature demodulations, where the receiver has two channels: in phase (I) and quadrature (Q). However, some design issues arise due to certain inherent characteristics of the direct conversion architecture, such as DC offset errors, I and Q mismatch, and even order harmonic distortion. DC offset issues have been examined in past thesis projects, such as the variable resolution direction finding (DF) using a Robust Symmetrical Number System (RSNS) [2] and the distributed digital array radar (DDAR) study [3]. Initial calibration of a direct conversion demodulator board is required in order to calculate the offset errors and compensate for the phase errors during beamforming and demodulation processing.

B. PREVIOUS WORK

The DC offset problem has proven to be critical in influencing the accuracy of angle of arrival (AOA) calculations of a RSNS virtual spacing direction finding system. Thus, there is previous work done by Benveniste [4] to calibrate the demodulation board prior to actual application in a RSNS system. The proposed demodulator board calibration station uses phase shifters to run through 37 step sizes, each at approximately 10^0 until all 360^0 of phase shift is covered. The recorded I and Q values were used to plot

out a circle and by averaging these values, the center of the circle can be calculated. Any I and Q offset values are passed on for use in the AOA calculation of the RSNS system.

The manual calibration station setup, as shown in Figure 2, consists of both hardware and software. Hardware consists of main components such as phase shifters, LO source at 2.4 GHz, power splitter, NI PXIe-1062Q computer, and uncalibrated demodulator boards [4]. For calibration of a single board, only one path is needed (one of the dashed boxes). A second path was added to this setup to allow for additional measurements between boards, such as phase synchronization.

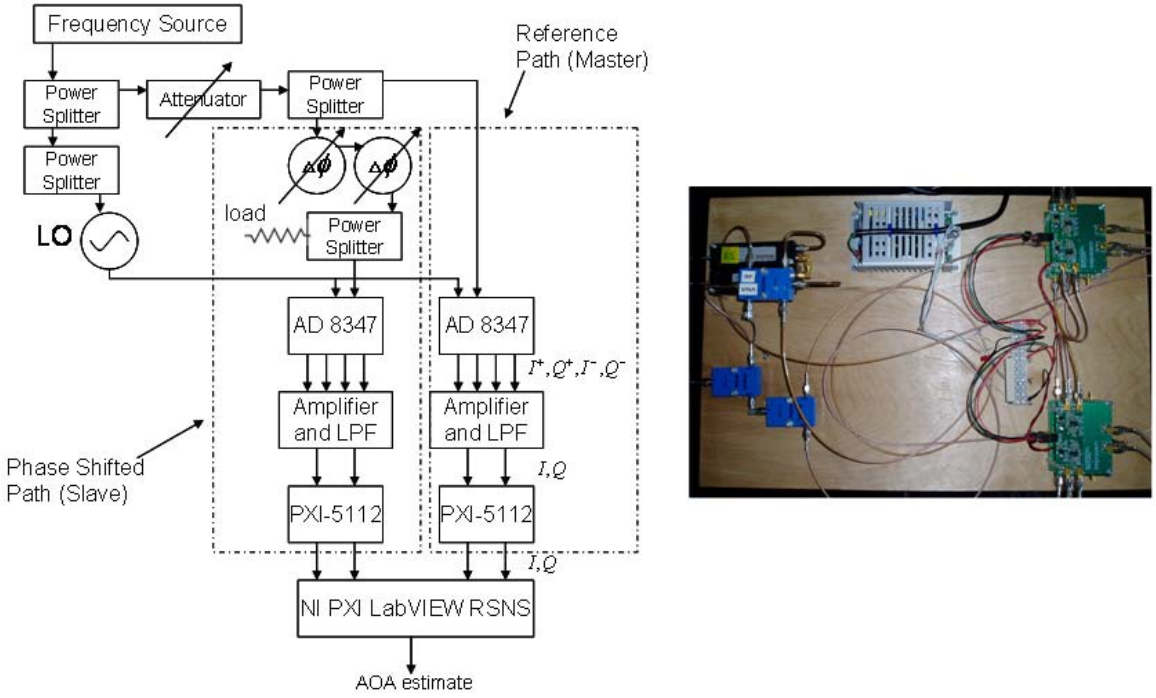

Figure 2. Laboratory Hardware Setup and Block Diagram (After: [4]).

As for the software portion, a LabVIEW calibration program was written to carry out two important tasks. The first is to create of a graphical user interface (GUI) for the user's control over the calibration process. The second is post processing of the recorded I and Q values.

The present manual calibration process begins with the LabVIEW calibration program running to take one record of I and Q data at a constant phase. The user sets the phase by either manually turning the phase shifter clockwise or counter-clockwise to the

maximum position before starting the program. The program records 10,000 samples at a time and calculates the mean I and Q values, which are then saved. The user continues by turning 2 rounds (~ 10^0) of the phase shift to change the phase and the process repeats until the full 360^0 of phase shift is completed. After the full 360^0 cycling of the phase shifter is completed, the uncalibrated IQ plots can be generated using the previously stored values of I and Q data. The I and Q offsets are computed and a final plot of the calibrated IQ plots centered at zero is carried out [4]. The I and Q offsets become part of the demodulator's unique performance data. When the demodulator is employed in a receiver system, the values are downloaded to the processor and used to correct for the offsets.

C. THESIS OBJECTIVE

The primary focus of this thesis is to design a new calibration station that automates the entire process without the need of manually turning the phase shifters. It aims to improve on the performance of previously implemented calibration station in areas such as ease of use, duration of test, accuracy, and repeatability. The major upgrade to the existing calibration station is the use of a AD8346 modulator to automatically introduce phase shifting in the RF signal sent to the demodulator. In addition to determining DC offsets, a number of other tests can be performed to check the demodulator specifications. It can also serve as a software development platform. The calibration network has components that are easily accessible, so modifications are possible for the purpose of breadboarding circuit designs. New National Instruments (NI) hardware can be substituted, for example, a higher speed analog-to-digital converter (ADC), for evaluation.

D. THESIS ORGANIZATION

Chapter II explains direct conversion system and discusses its pros and cons. The DC offsets errors and their cause and effect are further elaborated.

Chapter III explains the function of the proposed calibration station to calibrate DC offsets errors of the demodulator board.

Chapter IV explains the calibration procedures and software, validates the calibration station performance, and evaluates the conducted tests.

Chapter V contains a concluding discussion and suggestions for future research.

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II. THEORY AND ISSUES OF DIRECT CONVERSION

This chapter starts with a brief discussion of modulation and demodulation and introduces the in-phase (I) and quadrature (Q) representation. It also provides an overview on the direct conversion system and discusses its pros and cons. Further elaboration on DC offset errors and some common solutions to this error are covered as well.

A. MODULATION

1. Modulation Concept

Most often, modulation refers to the mixing of two signals together for frequency translation (upconversion or downconversion). One signal is the information signal at frequency f_m and contains the data or information to be modulated. The other signal is the carrier signal and its frequency is known as the carrier frequency f_c. Usually, the carrier frequency is much higher than the highest frequency component of the information signal. The carrier signal is provided by a local oscillator (LO) and therefore it is often simply referred to as the LO.

There are two forms of modulation, namely, double side band modulation and single side band modulation. As shown in Figure 3, double side band modulation is the mixing of the message and carrier signals that results in a translation of the message signal frequency. The message frequency simply shifted from its original frequency band to upper side bands $(f_c + f_m)$, and lower side bands $(f_c - f_m)$.

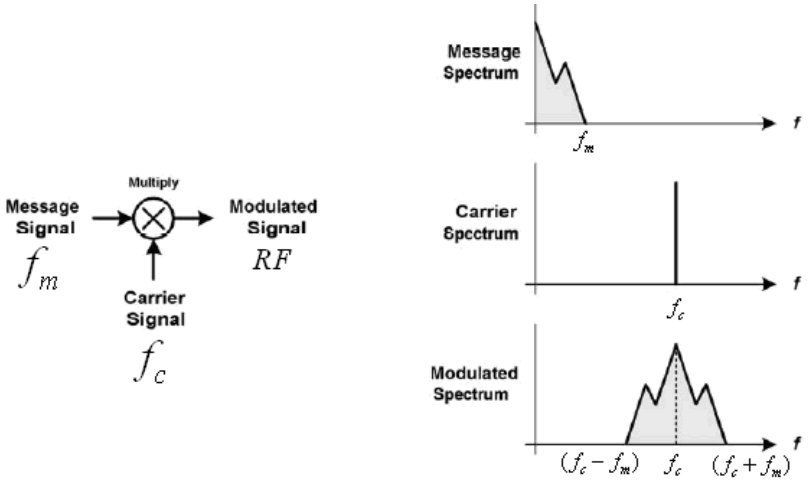

Figure 3. Double Side Band Modulator for Upconversion (After: [5]).

2. Quadrature Modulation and IQ Representation

The quadrature modulation scheme provides control of both phase and amplitude of a signal using a single modulator. However, the modulator consists of two channels, I and Q. I is the in-phase channel as the LO is in phase with a cosine reference, whereas Q is the quadrature channel as the LO is 90º phase shifted. The I and Q data can be used to represent the changes in the phase and amplitude of the modulated signal. Given the message IQ data, its information can be encoded onto this sine wave signal as a modulated signal. During the IQ modulation process, the carrier signal modulates (mixes) with this information signal causing phase and amplitude changes. We can easily extract the original information signal by reading the IQ data changes of the resulting modulated carrier signal. Thus, we can define modulation as the process in which a carrier signal phase, amplitude, or frequency changes according to the information signal containing the message data.

The general form of a modulated signal can be expressed as:

$$s(t) = A(t)\cos[\omega_c(t) + \phi(t)] \tag{2.1}$$

where *A(t)* is the time-varying amplitude, ω_c is the radian frequency of the carrier $(2\pi f_c)$ and $\phi(t)$ is the time-varying angle [6]. The in-phase and quadrature general form can be expressed as [7]:

$$s(t) = I(t)\cos(2\pi f_C t) - Q(t)\sin(2\pi f_C t) \tag{2.2}$$

where,

$$I(t) = A(t)\cos[\phi(t)] \tag{2.3}$$

$$Q(t) = A(t)\sin[\phi(t)] \tag{2.4}$$

The amplitude and phase represent a point on the I and Q plane, as shown in Figure 4.

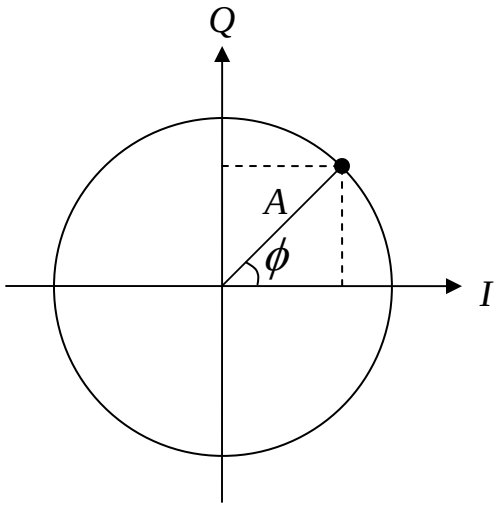

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Figure 4. The I (in-phase) and Q (quadrature) planes.

The phase is obtained from the quadrature components by

$$\phi(t) = \tan^{-1}[Q(t) / I(t)] \tag{2.5}$$

and the amplitude

$$A(t) = \sqrt{I(t)^2 + Q(t)^2} \tag{2.6}$$

The distance between the origin and a point (represented by a black dot) will remain constant as long as the amplitude remains the same. This will generate a circle that rotates in counter-clockwise direction around the origin as the phase of the RF carrier wave increases.

We can either implement expensive hardware circuitry to change the amplitude, phase, or frequency of a modulating RF carrier wave or simply change the amplitudes of I and Q input signal in Equation (2.2) . The latter proves to be a more flexible and cheaper option.

3. IQ Modulator

As shown in Figure 5, a typical IQ modulator has components such as a 90º phase shifter, an I mixer, a Q mixer and an RF subtracting/summing junction to produce a modulated RF signal. The two mixers are fundamentally frequency multipliers that up convert the message signal. For this case, we are using it for up converting (modulation), but the process can also be used for down converting (demodulation). One of the mixers multiply the I channel LO signal (cosine wave) with the RF carrier wave. The other multiplies the Q channel signal (sine wave due to a 90-degree phase shift) with the same RF carrier wave. The subtraction of the two gives the result as shown in Eq. (2.2). This modulation method is also known as quadrature upconversion due to the 90º phase shift of the RF carrier wave at one of the mixer inputs. This IQ modulator is commonly used for most designs because of its simplicity and flexibility in implementation of various modulation schemes [8].

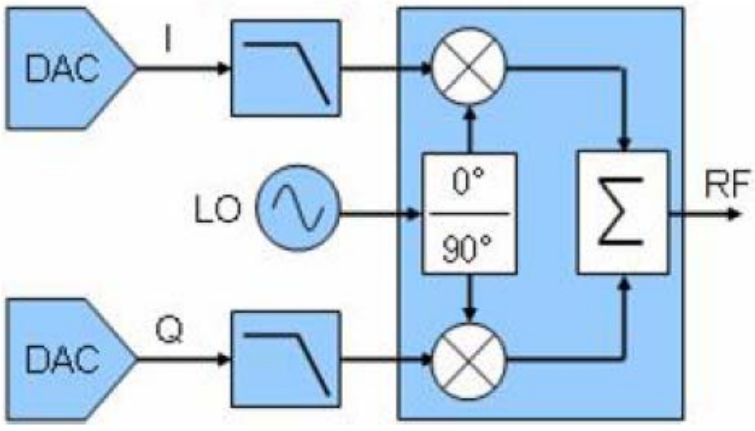

Figure 5. Hardware Diagram of Direct Upconversion Modulation (From: [1]).

4. Direct Upconversion

When the mixing frequency in Figure 5 is the final carrier frequency, the process is called the upconversion. The upconversion to the carrier frequency is shown with one stage, as opposed to going to an intermediate frequency (IF) first. Most often, in modern communication systems, it is done in a single stage. Direct conversion is also known as homodyne or zero-IF. It is one of the simplest frequency translation methods (fewer components) commonly used in RF communication devices. Direct conversion architectures can be easily integrated in a single circuit board and have fewer components than other methods. Thus, they are cost effective and simple to implement.

Translated into the frequency domain, the I and Q baseband signals (centered at zero frequency) are shifted to an RF signal as shown in Figure 6, where the I and Q signals mix with an LO signal at the center frequency of the RF signal. Each baseband I and Q signal is equivalent to half the bandwidth of the RF signal.

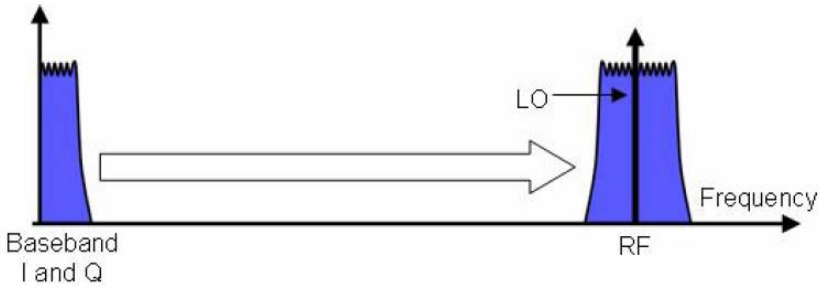

Figure 6. Frequency Domain of Upconverting to RF (From: [1]).

B. DEMODULATION

1. Demodulation Concept

Demodulation is the inverse of modulation whereby the original message signal is downconverted and recovered by means of translating the baseband signal from the modulated RF signal as shown in Figure 7. The process mainly involves the use of a mixer that is a frequency converter, mixing the carrier frequency (LO) with the RF signal to recover the baseband signal or message signal.

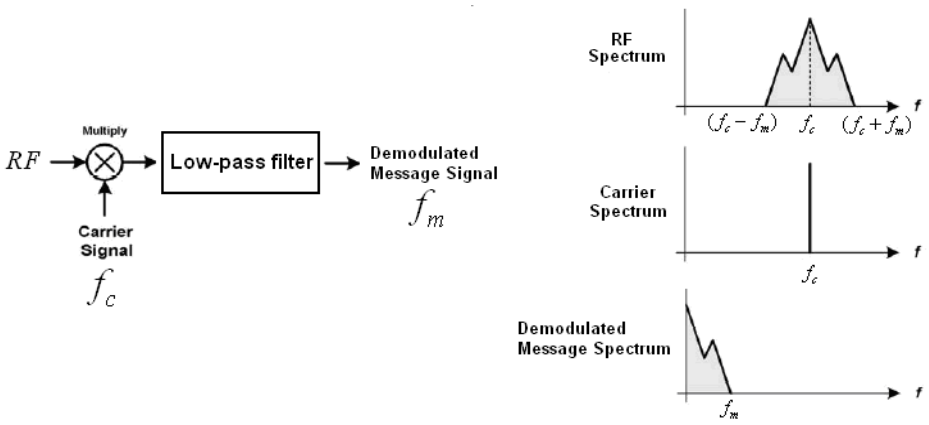

Figure 7. Single Channel Demodulator for Downconversion (After: [5]).

2. Direct Downconversion (Homodyne) Demodulation

As illustrated in Figure 8, a direct downconverter uses two analog signal mixers to mix the modulated RF signal with the LO. The LO signal is split into a 0^0 phase LO signal ($\cos\omega_c t$) and the other into a 90^0 out of phase LO ($\sin\omega_c t$) for mixing with the RF signal. The resultant output from the mixers are the baseband I and Q signals that are further filtered by low pass filters before being converted into digital signals by the analog-to-digital converter (ADC).

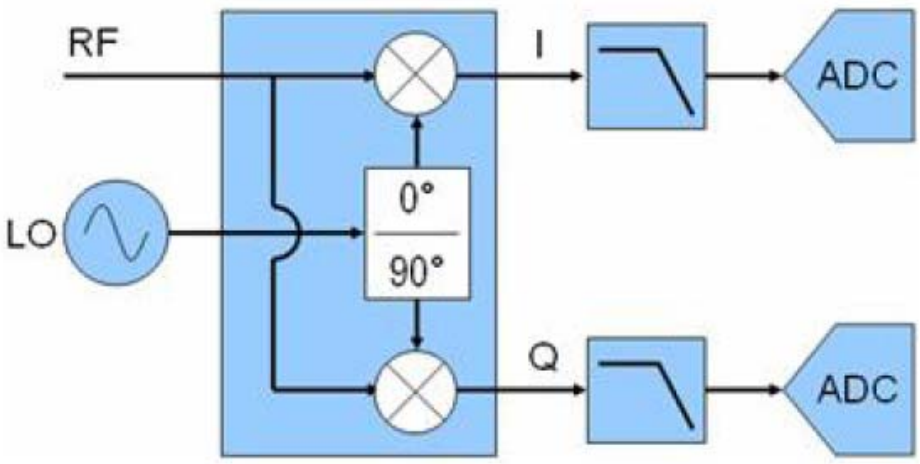

Figure 8. Direct Downconversion Receiver (From: [1]).

The process demodulates by shifting the received RF signals directly into the baseband as shown in Figure 9, using a local oscillator having a similar frequency as the received RF signal. This process recovers the original baseband signal that was modulated with the LO at a higher frequency during the modulation process. The information or message can then be decoded from the I and Q components.

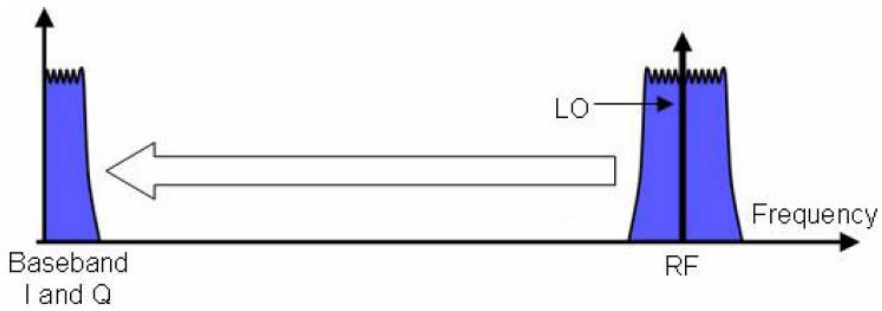

Figure 9. Frequency Domain of Downconverting back to Baseband (From: [1]).

Thus, homodyning efficiently allows the conversion of RF signals to baseband directly, unlike a heterodyne design that needs intermediate frequency for conversion. This eliminates the need for extra IF related circuitry, indirectly reducing the overall cost and power consumption.

3. Direct Conversion (Homodyne) Issues

Although there are technical and monetary advantages to the direct conversion system, it does have other technical issues that are inherent in the design. Drawbacks such as DC offsets, I/Q mismatch, even-order distortion, flicker noise and LO leakage [9] should be part of the design consideration. The following sections give an overview of the issues associated with RF direct conversion.

(a) DC Offsets

DC offset refers to the displacement of the IQ circle in Figure 4 from the origin. Eliminating DC offset is critical as it causes errors in the final demodulated signal, analog-to-digital converter saturation that limits dynamic range, and extra power consumption [10]. There are a couple of contributing factors such as implementation of

IQ mixers and self-mixing phenomenon caused by LO or interferers [9]. The next section (Section C) will further elaborate on its effects and various methods of mitigating the effect of offsets.

(b) I/Q Mismatch

I/Q mismatch refers to phase and gain imbalance between the in-phase and quadrature signal paths. Ideally, the phase difference between local oscillator (LO) signals of the I and Q channels is orthogonal, but causes a I/Q mismatch when not [11]. To illustrate the effects of mismatch effects, suppose the received signal is [9] :

$$r(t) = a\cos\omega_c t + b\sin\omega_c t \tag{2.7}$$

where a and b are either -1 or +1. The I and Q phases of the LO signals can be represented as:

$$I_{LO}(t) = 2\cos\omega_c t \tag{2.8}$$

$$Q_{LO}(t) = 2(1+\varepsilon)\sin(\omega_c t + \theta) \tag{2.9}$$

where the factor 2 is included to simplify the results, ε is the gain error and θ is the phase error. After multiplying $r(t)$ in Equation (2.7) by the LO signals and low-pass filtering the result will yield the baseband signals as:

$$I(t) = a \tag{2.10}$$

$$Q(t) = (1+\varepsilon)b\cos\theta - (1+\varepsilon)a\sin\theta \tag{2.11}$$

Gain error transforms as a nonunity scale factor in the amplitude, leading to amplitude errors [9]. This amplitude error causes the original IQ circle to translate into an ellipse as shown in Figure 10 [12].

Phase imbalance causes corruption of each other's channel (I and Q) and the signal-to-noise ratio (SNR) degrades if the I and Q data streams are uncorrelated [9].

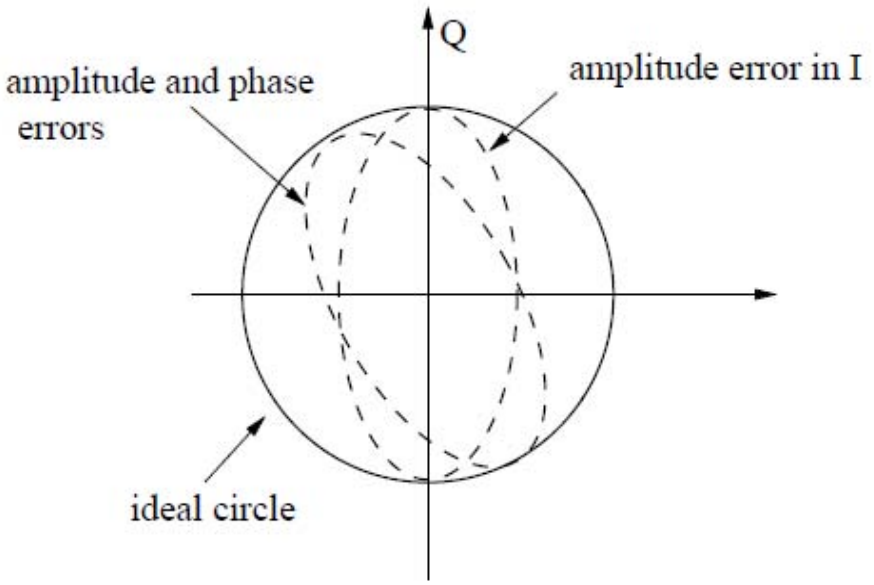

Figure 10. Effects of Amplitude and Phase Errors (After: [12]).

The effects of IQ gain errors and phase imbalance are more critical in higher order modulation schemes such as 64-QAM as demonstrated by the diagrams shown in Figure 11 and Figure 12. Because IQ errors will cause the constellation plots to spin, the demodulator is unable to estimate correctly the base band signal phase or frequency. Thus, a higher modulation scheme is more sensitive to error, and it can prevent the recovery of the carrier signal during demodulation. A few dBs of error causes enough corruption so that demodulation is not possible [1].

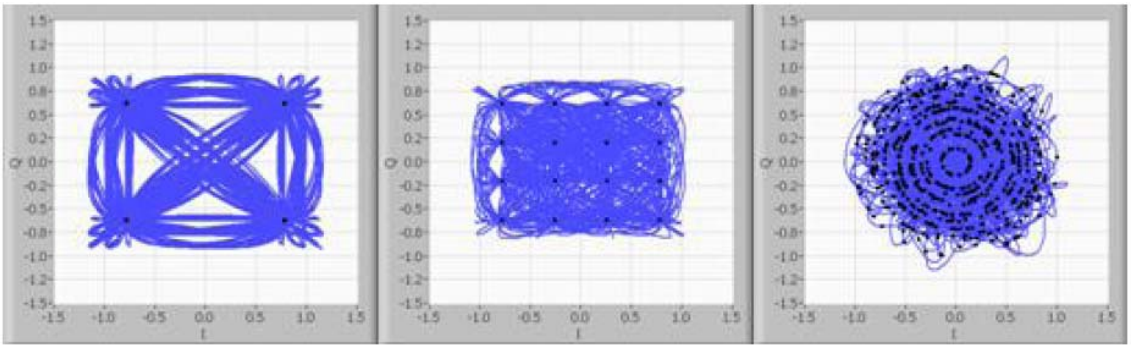

Figure 11. IQ Gain Errors in 4-QAM, 16-QAM and 64-QAM Signals (From: [1]).

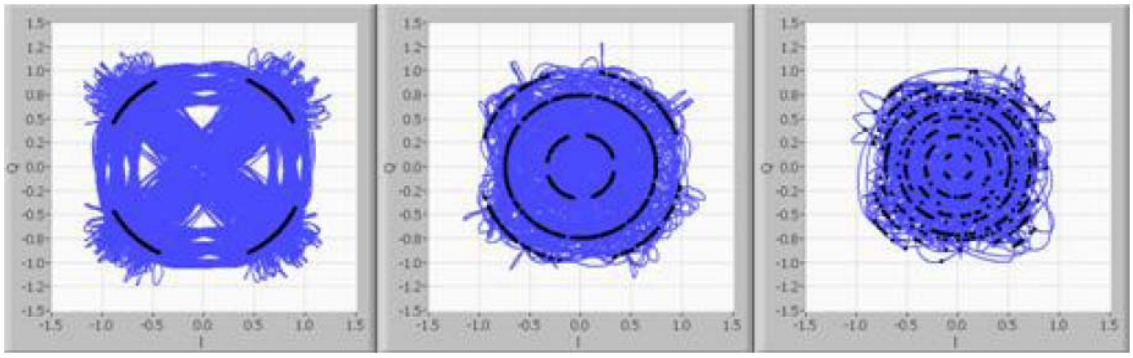

Figure 12. Phase Imbalance in 4-QAM, 16-QAM, 64-QAM Signals (From: [1]).

IQ mismatch is known to be less problematic in direct conversion receivers than other architectures. A 5-degree phase imbalance degrades the SNR by roughly 1 dB [9]. Nevertheless, there are multiple analog and digital solutions to IQ mismatch. An analog solution is designing the original circuitry with some careful component layout in order to make the circuit more robust. Digital solutions include applying a Hilbert transform to generate I/Q signals in the digital domain and then using adaptive mismatch cancellation systems or replacing analog-to-digital converter with delta-sigma modulator [13].

Figure 13 demonstrates the effect of DC offsets that lead to phase error. There are two IQ circles, one being uncalibrated (displaced from the origin) and the other calibrated (centered at the origin).

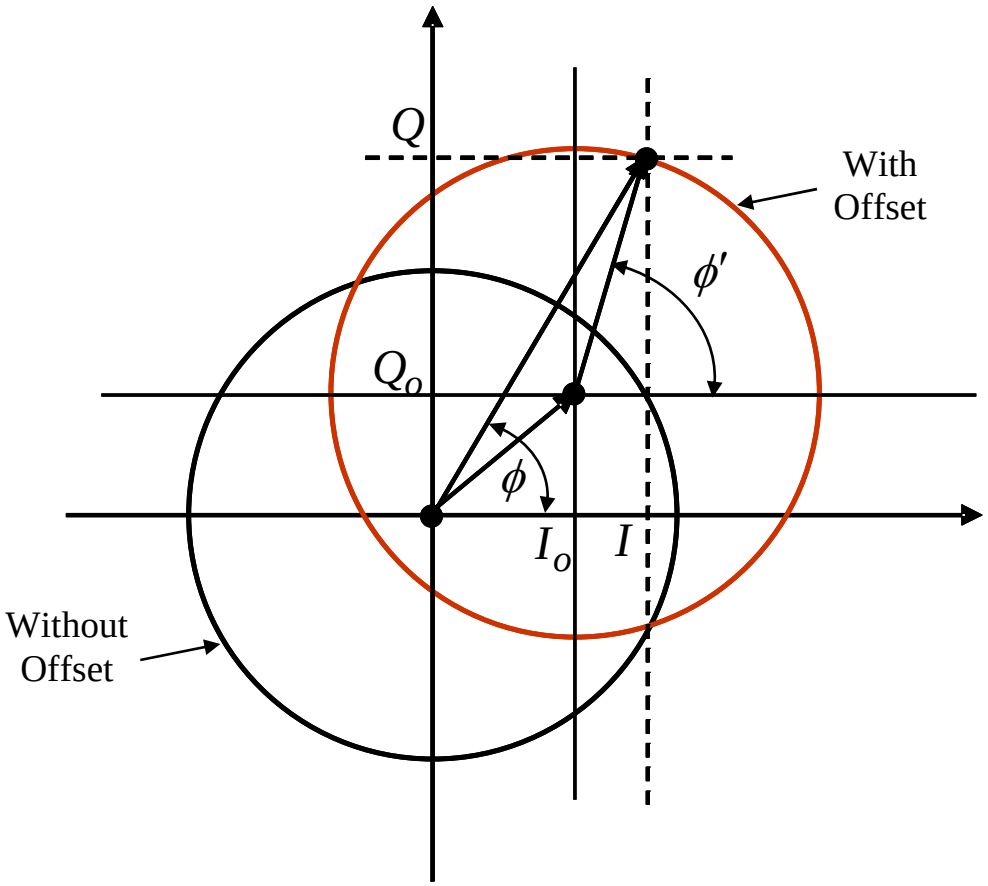

Figure 13. IQ circle - Phase Error due to DC Offsets.

The uncorrected phase (ϕ) can be calculated using

$$\tan\phi = Q / I \tag{2.12}$$

where I and Q are the raw I and Q data. The corrected phase (ϕ') can be calculated using

$$\tan\phi' = (Q - Q_O) / (I - I_O) \tag{2.13}$$

where I_O and Q_O are the DC offsets of the uncalibrated circle (raw data). Thus the phase error due to DC offset can be calculated by taking the difference between ϕ and ϕ'

$$\text{phase error} = \phi - \phi' \tag{2.14}$$

The I and Q measurements from a calibration test are shown in Figure 14. The raw uncalibrated data is shown on the left and the calibrated (offsets removed) is on the right. The two circles are shown together in Figure 15. Also shown in the same figure is

the phase error from Equation (2.14). Clearly, from the phase error plot, compensation for the offsets is necessary to maintain phase errors below 20 degrees or so.

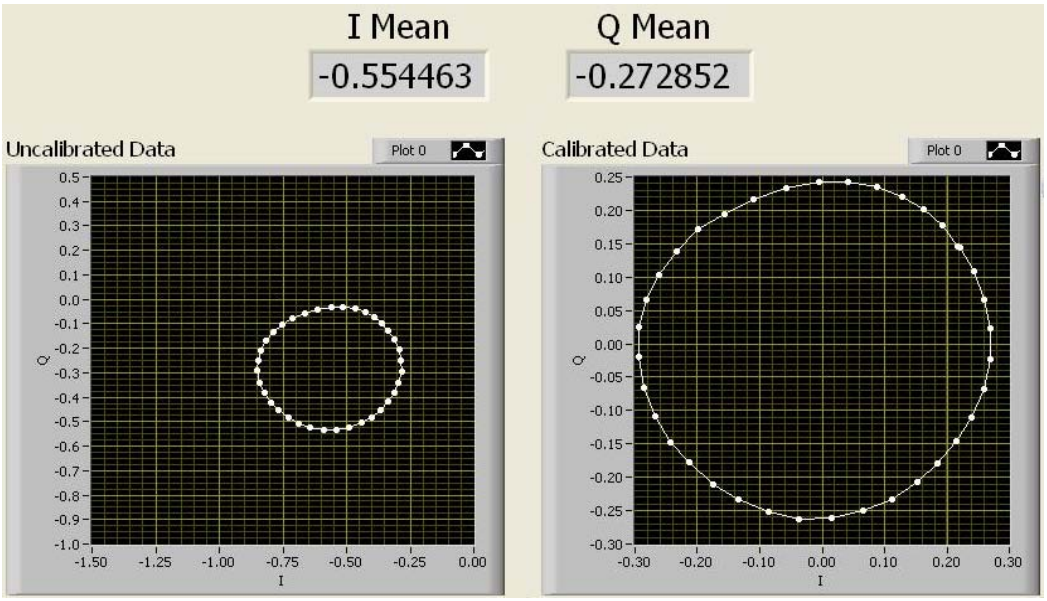

Figure 14. Calibration Test Measurements - Raw Data.

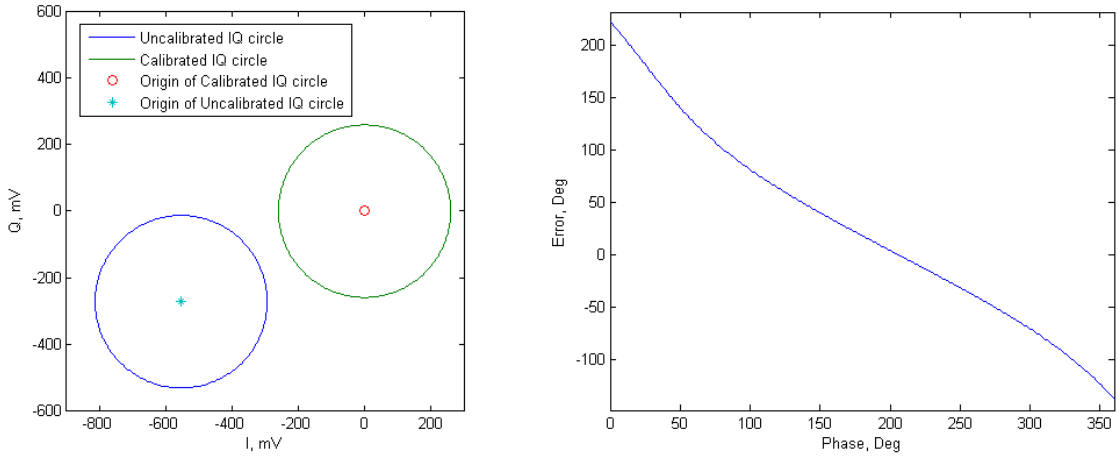

Figure 15. Plot of DC Offsets (left) and Plot of Phase Error (right).

(c) Even-Order Distortion

Direct conversion is more sensitive to even-order distortion. As shown in Figure 16, two high frequency interferers near a particular desired channel have a nonlinearity in

the LNA, generating a low-frequency term due to an even-order distortion. In an ideal mixer scenario, this unwanted low-frequency term can be ignored, as it will be transformed into high-frequency components through the mixer multiplication process. However, in reality, mixers have a finite direct feedthrough (signal passes through with finite attenuation from RF input to output) characteristics, thus causing errors to the final downconverted signal [9].

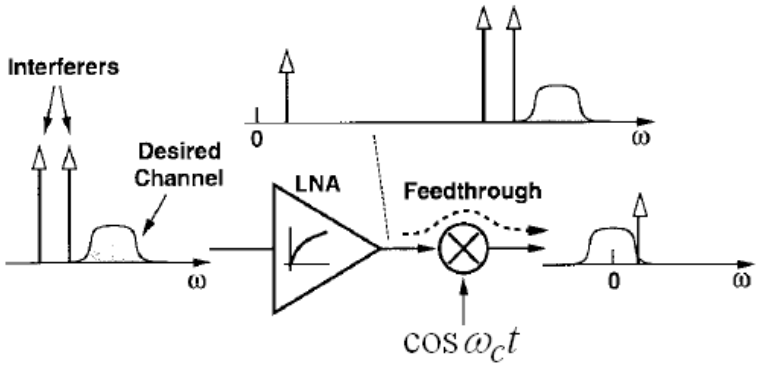

Figure 16. Effect of Even-Order Distortion on Interferers (From: [9]).

The second harmonic of the desired RF signal is another problem of second-order nonlinearity. As shown in Figure 17, this particular order of harmonic can be downconverted to the baseband if mixed with the second harmonic of the LO output. It has a similar effect with higher order harmonics, but it will not be critical in differential mixers because the harmonics and magnitudes of both the RF signal and the LO are inversely proportional to the frequency [9].

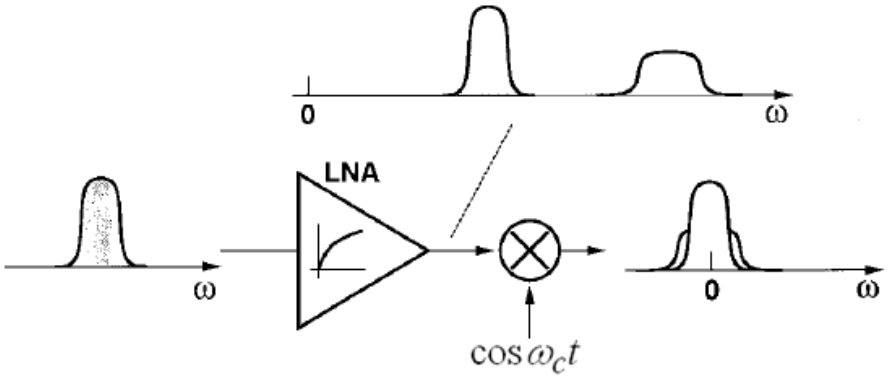

Figure 17. Downconversion of Signal Harmonics (From: [9]).

The second order nonlinearity characteristics can often be found in most data sheets, listed as IP2 or the “second intercept point”. The IP2 characteristics graph is plotted by extrapolating the results of plotting the unwanted low frequency signal power of two equal-amplitude interferers at the input versus the input power [9].

There are some hardware solutions to reducing this non-linearity, such as highly improved IP2 direct conversion receiver [14]. The circuit design is based on three, instead of two, mixers for recovering the in-phase and quadrature components of bi-dimensional modulated signals. Another solution is to suppress the resulting low-frequency component directly after the mixer has a non-linearity effect [9].

(d) Flicker Noise

The downconverted demodulated signal is usually small, in the range of tens of microvolts, assuming a typical gain of about 30 dB in the LNA/mixer combination. Thus, the input noise at amplifiers and filters stages is an important parameter to control. The noise of devices, such as a MOFET transistor (amplifier) has a profound effect on the signal integrity, especially when the downconverted frequency spectrum is located near zero frequency. The flicker noise effect (also known as $1/f$ noise) can be minimized with a different mix of methods. Designers can opt to use larger devices (several thousand microns wide) to minimize the amplitude of the flicker noise as the subsequent stages following the mixer are operating at low frequencies. Other methods such periodic offset cancellation can also minimize the low frequency interferences using correlated double sampling [9].

(e) LO Leakage

LO signal leakage to the antenna will radiate, scatter from objects in the environment, and then be received causing interference in addition to onboard leakage. Heterodyne and image-reject mixers are less problematic as their LO frequency is often out of the reception band. Fabricating more parts of RF transceivers on the same chip can minimize the issues of LO signal leakage. The antenna net coupling can also be minimized to acceptable low levels with differential local oscillators in the receiver [9].

C. DC OFFSET

DC offset occurs in both the modulation and demodulation processes. As explained earlier, DC offset is an unwanted offset voltage that will corrupt the actual information and cause the ideal IQ circle to translate away from the origin of the IQ plot as shown in Figure 18.

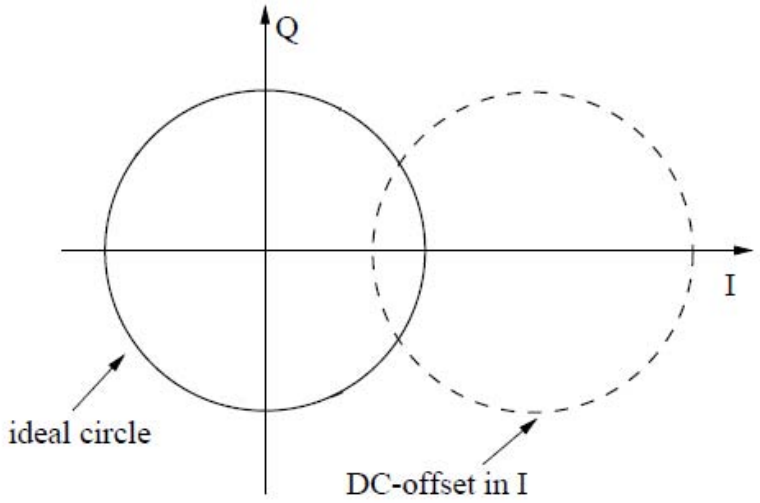

Figure 18. Resultant DC-Offset (After: [12]).

1. DC Offset in Direct Upconversion Modulation Process

DC offsets may be generated by the digital-to-analog converter (DAC) and/or the low pass filter (LPF) as shown in Figure 19. The DAC basically converts the incoming digital signal into an analog form that is passed on to the low pass filter to be converted into a filtered analog signal. Next, this filtered analog signal will be modulated onto a carrier by the modulator [15]. Thus, any DC offset errors introduced at the DAC will be propagated from the start of the DAC process until the final modulation path as a modulated RF signal. This is due to the amplitude of each I and Q vector phase of the baseband signal that is translated to the amplitude and frequency of this final modulated RF signal [1].

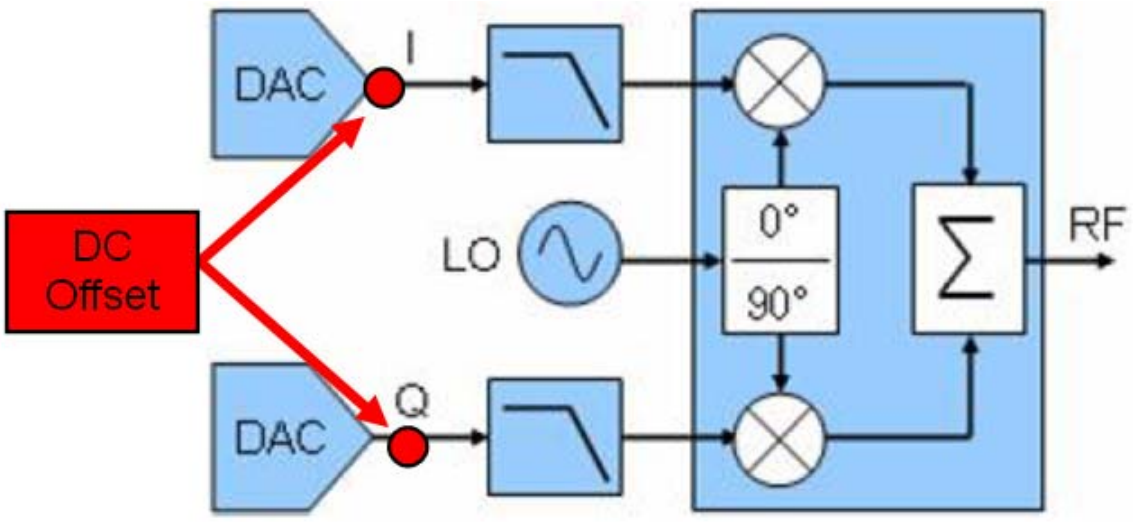

Figure 19. DC Offset Error in a Direct Upconversion Transmitter (After: [1]).

The graph in Figure 20 shows a plot of two baseband signals, I and Q (I in red, Q in blue) in the time domain. I and Q signals are required to be accurately synchronized and sampled at appropriate intervals during a demodulation process of recovering the actual symbols [1].

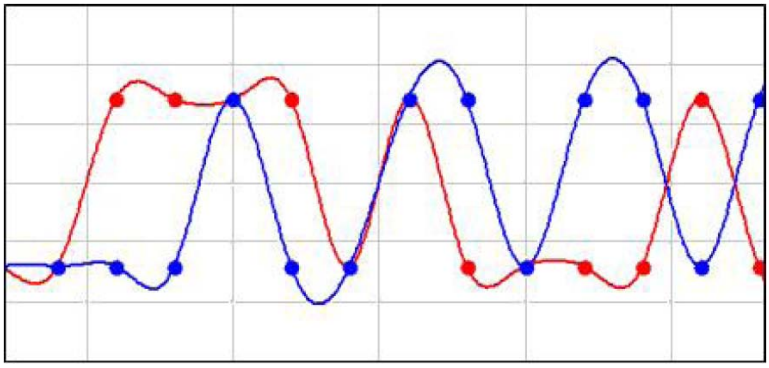

Figure 20. Graph of a Baseband Signal (From: [1]).

The dots on the waveform of both I and Q signals represent the ideal symbol locations for the given baseband signals in time domain. The DC offsets errors will affect the baseband signal accuracy in terms of amplitude, phase, and frequency, thus recovering erroneous symbols during demodulation [1].

Different types of modulation schemes have different tolerances towards DC offsets. For example, a simpler modulation scheme such as 4-QAM or BPSK demonstrates a higher resilience towards inaccurate baseband signals caused by DC offsets than do higher order modulation schemes such as 64-QAM and 256-QAM. Figure 21 illustrates three constellation plots based on 4-QAM, 16-QAM, and 64-QAM during demodulation process where both baseband I and Q signals had a 10% DC offset. It was observed that the demodulation algorithm had caused the constellation plot to spin due to the inaccurate estimation of the phase or frequency of the baseband signal [1].

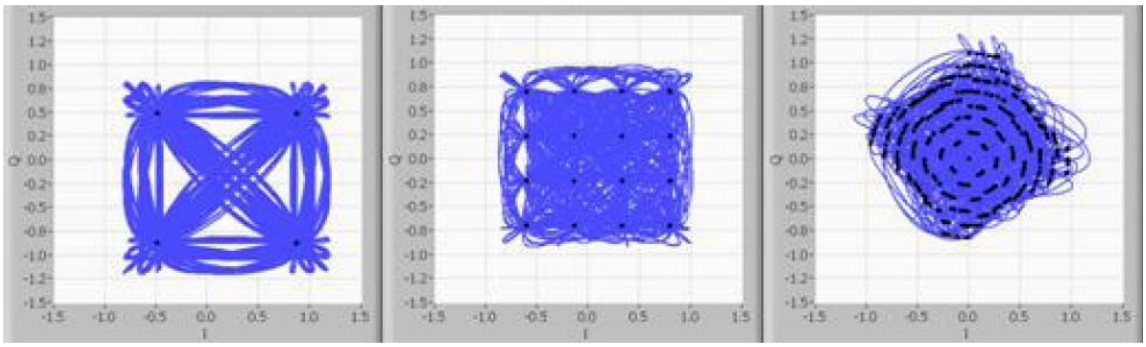

Figure 21. DC Offset in 4-QAM, 16-QAM, 64-QAM Signals (From: [1]).

There are various mitigations and solutions to the problems mentioned above, such as using a high performance DAC and tight tolerance passive filter, but they are not economical as these are expensive and complicated solutions to remove the DC offset. An example of a practical implementation is using a DC offset compensator that reduces the DC offset to within acceptable limits for the modulation that is used. It has a sensor that detects the error in the filtered analog signal after the low pass filter and compensates for it [15]. When used in digital beamforming, it is possible to remove any offsets from the sampled data before processing.

2. DC Offset in Direct Downconversion Demodulation Process

A demodulated signal can also be corrupted by DC offset voltages during a direct downconversion process as the downconverted baseband signal extends into the zero frequency band. Thus, this unwanted voltage (in the form of DC offset) at this zero

frequency band corrupts the actual signal. DC offsets can be induced through a phenomenon called “Self Mixing,” either by the LO leakage or interferer leakage, as shown in Figure 22 and Figure 23 respectively [9].

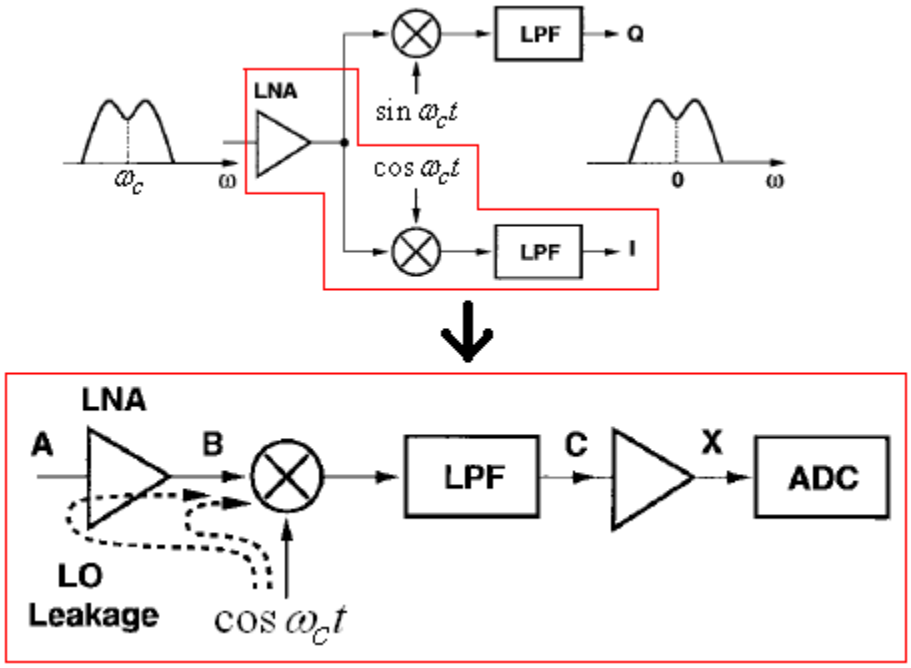

Figure 22. Self-Mixing of LO Leakage in Direct Down Conversion (After: [9]).

Self-mixing of LO leakage, as in Figure 22, occurs due to the inherent characteristics of the isolation between the LO, mixer, and Low Noise Amplifier (LNA). As this isolation is not effective enough to provide total isolation, a finite amount of feedthrough known as “LO Leakage” leaks from LO to point A and B. This LO leakage is caused by coupling effects, such as capacitive coupling, substrate coupling. and bond wire coupling, when LO signal is provided externally. Therefore, a DC offset component exists at point C when the LO signal leaking through to inputs of the LNA (point A) and the mixer (point B) is mixed with the LO signal [9].

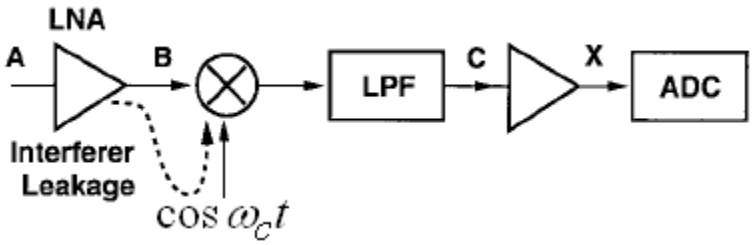

Figure 23. Self-Mixing of Interferers (After: [9]).

Self mixing of an interferer's leakage, as in Figure 23, occurs when large amount of external interference leaks from the LNA at point A or mixer input to the LO port, causing a mixer multiplication effect [9].

Gain at the LNA/mixer can also amplify the DC offset beyond a level where it is more than 300 times (e.g. 10 mV versus 30 μV) the desired signal level. Subsequently, amplification continues from point C to point X, in which the DC offset voltage further saturates the circuitry and prevents the amplification of the desired signal [9].

The situation whereby self-mixing varies with time may worsen the DC offset problem. This situation happens when LO leakage to the antenna is illuminating a moving object (e.g., a car moving at high speed) and then is scattered back to the receiver [9].

There are possible solutions such AC coupling and offset cancellation in reducing or cancelling the DC offsets. In the case of AC coupling, a high pass filtering is used in the downconverted signal path. As for offset cancellation, it uses a capacitor to store the offset during the idle mode and subtract it from the signal during the actual receiving mode as shown in Figure 24 for a time-division multiple access (TDMA) system [9].

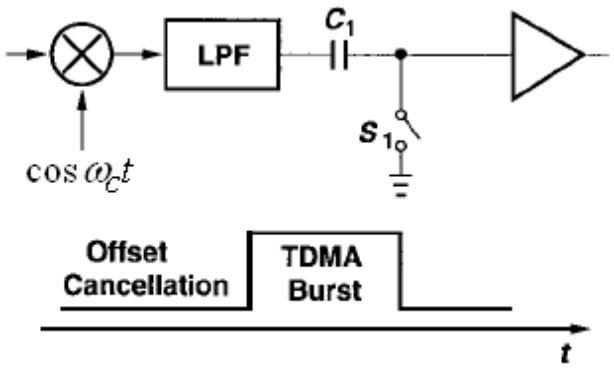

Figure 24. Offset Cancellation in a TDMA System (From: [9]).

D. SUMMARY

In this chapter, a short discussion on in phase (I) and quadrature (Q) representation of modulation and demodulation was discussed. Also discussed were the pros and cons of a direct conversion system and how inherent DC offsets errors affects the system performance during implementation. In the next chapter, the architecture of an automated calibration station is introduced.

III. SYSTEM ANALYSIS OF THE AUTOMATED CALIBRATION STATION

This chapter describes the automated calibration station that was designed with the objective of improving the previously implemented manual calibration station. Targeted areas of improvement include automating the entire process without the need of manually turning the phase shifters for ease of use, decreasing the duration of the overall calibration process, and improving the accuracy of the post calibration DC offset results by using averaging of multiple tests on a single demodulator board.

A. PROPOSED ARCHITECTURE

For improving the ease of use, it was decided to automate the process of doing the phase shifting by replacing the phase shifter with a AD8346 quadrature modulator card. Figure 25 illustrates the block diagram of the test station architecture.

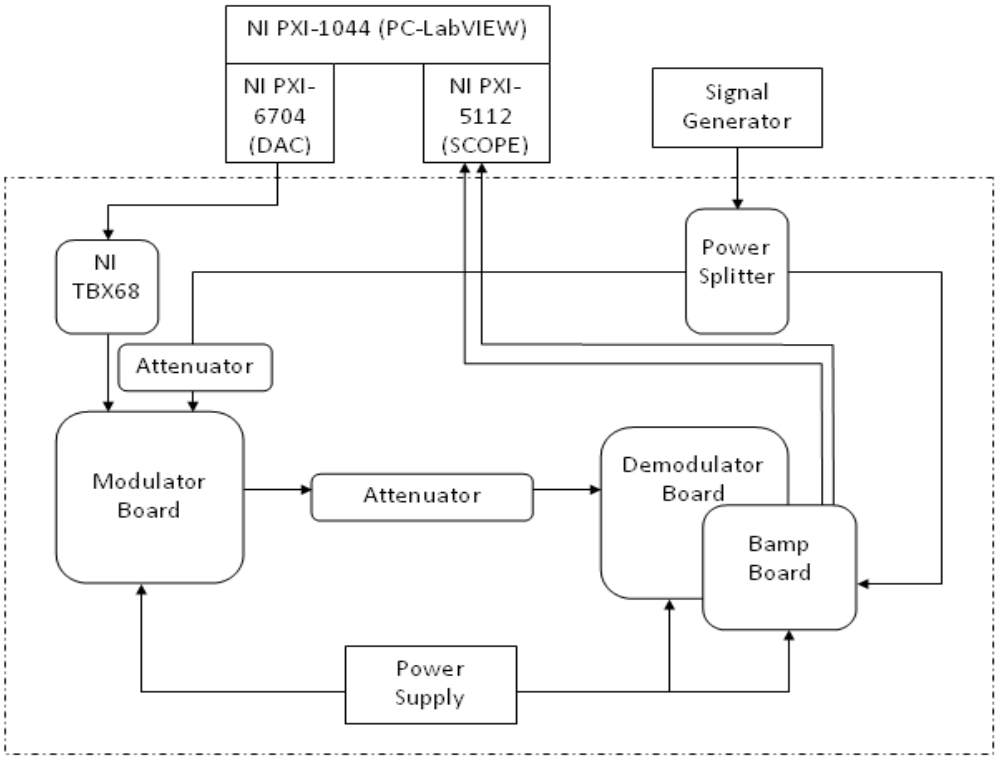

Figure 25. Block Diagram of Calibration Station.

I and Q signals are digitally generated with a combination of hardware and software, such as NI PXI-1044 chassis and computer and LabVIEW program. The LabVIEW program cycles through 37 steps of 10^0 phase shift over a range of 0^0 to 360^0. These signals are converted into analog outputs using NI PXI-6704 DACs. Subsequently, these converted analog signals are fed into the modulator, going through an upconversion modulation process with an RF output. This RF output is further attenuated to meet the RFIN specification of the quadrature demodulator before feeding into the board to recover the four differential I and Q control signals (IP, IN, QP, QN). The Bamp board converts these four control signals into two I and Q signals and amplifies them before feeding into the NI PXI-5112, which is a digitizer for capturing I and Q signals. After the full cycling (360^0) of phase shifting by the modulator is completed, I and Q offsets are computed and a final plot of the calibrated IQ plots centered at zero is carried out. This calibrated plot can be compared against an uncalibrated IQ plots generated using the stored I and Q uncorrected values. This completes the cycle of the calibration process.

B. DESCRIPTION OF HARDWARE COMPONENTS

1. Modulator Board

The main function of the modulator board is for phase shifting of the RF signal, replacing the need for a manually turned phase shifter. The selected modulator board is the AD8346 manufactured by Analog Devices, which had been investigated in past research [16-18]. In [16], various tests were conducted to test the phase shifting properties of the modulator card and results were satisfactory. However, there were some inherent phase errors of $\pm 2.5^o$. Some characteristics of the AD8346 modulator were also investigated in [17] and [18] such as the bandwidth characteristics (i.e., phase versus frequency response, and amplitude versus frequency response), output power characteristics for range of differential I/Q inputs at a set of fixed LO frequencies, etc.

The AD8346 evaluation board is shown in Figure 26, which illustrates the various connections to the board.

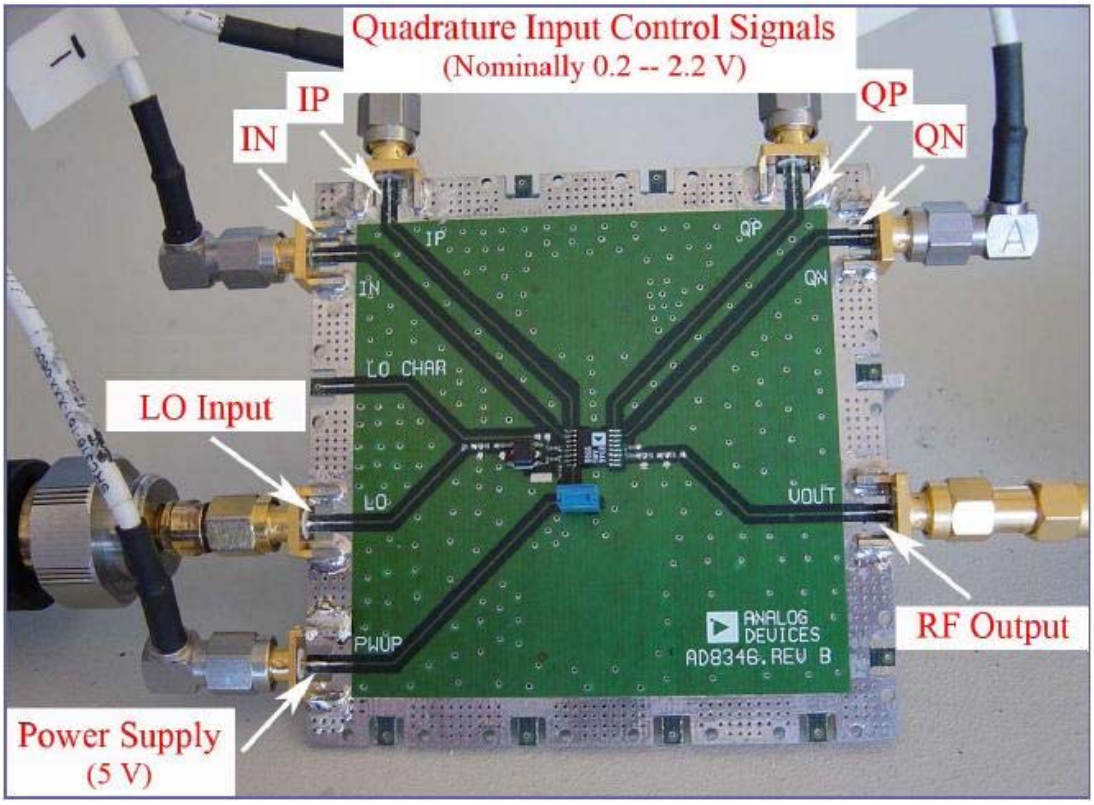

Figure 26. AD8346 Evaluation Board Wiring Connections (From: [18]).

The board has four quadrature input control signals labeled as In-phase negative (IN), In-phase positive (IP), Quadrature positive (QP) and Quadrature negative (QN). The output I and Q baseband signal modulated on RF output signal can be derived from:

$$I = I^{+} + I^{-} \tag{3.1}$$

$$Q = Q^{+} + Q^{-} \tag{3.2}$$

As in [16] and [17], positive voltage was applied to the negative input pin for phase shifting purposes when generating negative value of either I or Q is needed. The phase shift quadrant determines which two pins receive control voltage signals, while the other two are set to zero volts as shown in Figure 27. Thus, this method did not optimize the use of the differential properties of the four inputs on the modulator card.

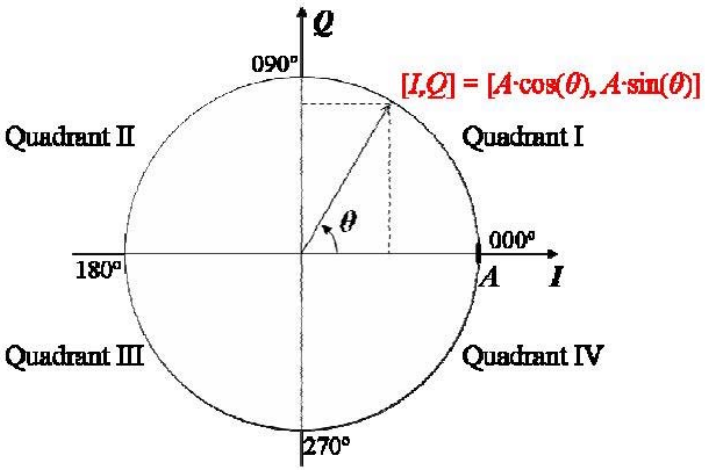

Figure 27. Typical Complex Phasor Plane (From: [18]).

As such, the modulator card must be optimized by applying the necessary voltages across four differential input control signals (IP, IN, QP, QN) [18]. The recommended differential input control signals should be dc biased to approximately 1.2 V based on AD8346 data sheets [19]. Next, the differential I/Q channel baseband input control signals were implemented using the following relationships:

$$IP(\theta) = 1.2 + \frac{1}{2} I(\theta) \tag{3.3}$$

$$IN(\theta) = 1.2 - \frac{1}{2} I(\theta) \tag{3.4}$$

$$QP(\theta) = 1.2 + \frac{1}{2} Q(\theta) \tag{3.5}$$

$$QN(\theta) = 1.2 - \frac{1}{2} Q(\theta) \tag{3.6}$$

Using Equations (3.3) to (3.6), the maximum differential input control signal voltage calculated is 2.4 V for an I and Q circle with 1.2 V radius. This is below the recommended maximum voltage of 2.5 V based on AD8346 data sheets [19].

For the calibration station setup, a LabVIEW program was written to implement Equations (3.3) to (3.6), generating the necessary differential input control signals to the

modulator card. Table 1 illustrates the calculated I and Q signals required for generation of the desired phase, which are then used to calculate and generate the resultant four differential input control signals.

Desired Phase, θ_{set} [°]	$I(\theta)$ [V]	$Q(\theta)$ [V]	$IP(\theta)$ [V]	$IN(\theta)$ [V]	$QP(\theta)$ [V]	$QN(\theta)$ [V]
0	2.000	0.000	2.200	0.200	1.200	1.200
10	1.970	0.347	2.185	0.215	1.374	1.026
20	1.879	0.684	2.140	0.260	1.542	0.858
30	1.732	1.000	2.066	0.334	1.700	0.700
40	1.532	1.286	1.966	0.434	1.843	0.557
50	1.286	1.532	1.843	0.557	1.966	0.434
60	1.000	1.732	1.700	0.700	2.066	0.334
70	0.684	1.879	1.542	0.858	2.140	0.260
80	0.347	1.970	1.374	1.026	2.185	0.215
90	0.000	2.000	1.200	1.200	2.200	0.200
100	-0.347	1.970	1.026	1.374	2.185	0.215
110	-0.684	1.879	0.858	1.542	2.140	0.260
120	-1.000	1.732	0.700	1.700	2.066	0.334
130	-1.286	1.532	0.557	1.843	1.966	0.434
140	-1.532	1.286	0.434	1.966	1.843	0.557
150	-1.732	1.000	0.334	2.066	1.700	0.700
160	-1.879	0.684	0.260	2.140	1.542	0.858
170	-1.970	0.347	0.215	2.185	1.374	1.026
180	-2.000	0.000	0.200	2.200	1.200	1.200
190	-1.970	-0.347	0.215	2.185	1.026	1.374
200	-1.879	-0.684	0.260	2.140	0.858	1.542
210	-1.732	-1.000	0.334	2.066	0.700	1.700
220	-1.532	-1.286	0.434	1.966	0.557	1.843
230	-1.286	-1.532	0.557	1.843	0.434	1.966
240	-1.000	-1.732	0.700	1.700	0.334	2.066
250	-0.684	-1.879	0.858	1.542	0.260	2.140
260	-0.347	-1.970	1.026	1.374	0.215	2.185
270	0.000	-2.000	1.200	1.200	0.200	2.200
280	0.347	-1.970	1.374	1.026	0.215	2.185
290	0.684	-1.879	1.542	0.858	0.260	2.140
300	1.000	-1.732	1.700	0.700	0.334	2.066
310	1.286	-1.532	1.843	0.557	0.434	1.966
320	1.532	-1.286	1.966	0.434	0.557	1.843
330	1.732	-1.000	2.066	0.334	0.700	1.700
340	1.879	-0.684	2.140	0.260	0.858	1.542
350	1.970	-0.347	2.185	0.215	1.026	1.374
360	2.000	0.000	2.200	0.200	1.200	1.200

Table 1. Calculated Differential Input Control Signals (After: [18]).

2. Demodulator Board

The demodulator board is the main device under test (DUT), as calibration of the demodulator board is needed prior to its use in any receiving platform, such as the RSNS Direction Finder [4]. This board was proven to be a critical component of the overall system used for phase measurement. However, the negative part of this direct conversion (homodyne) demodulator board is that it has an inherent DC offset that will cause an error, resulting in inaccurate AOA calculation of the RSNS Direction Finder.

The function of the demodulator board is to demodulate or down convert the received RF signal to I and Q baseband signals by mixing with the LO signal as shown in Figure 28.

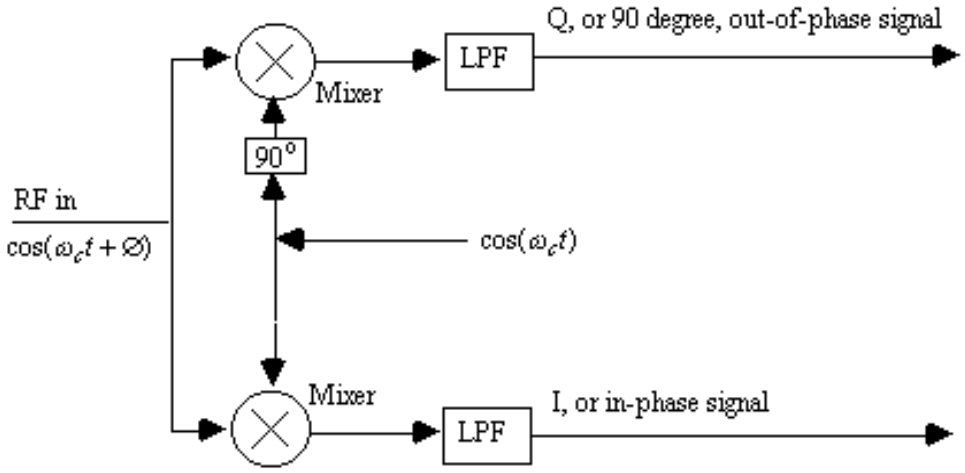

Figure 28. Quadrature Demodulator (From: [20]).

There are two modes of controlling the gain of the RF Variable Gain Amplifiers (VGA) namely, Automatic Gain Control (AGC) mode and VGIN mode. AGC mode has been implemented using the configuration option table in [21], where some of the connections on the board such as LK2 an LK6 shown in Figure 29 are shorted.

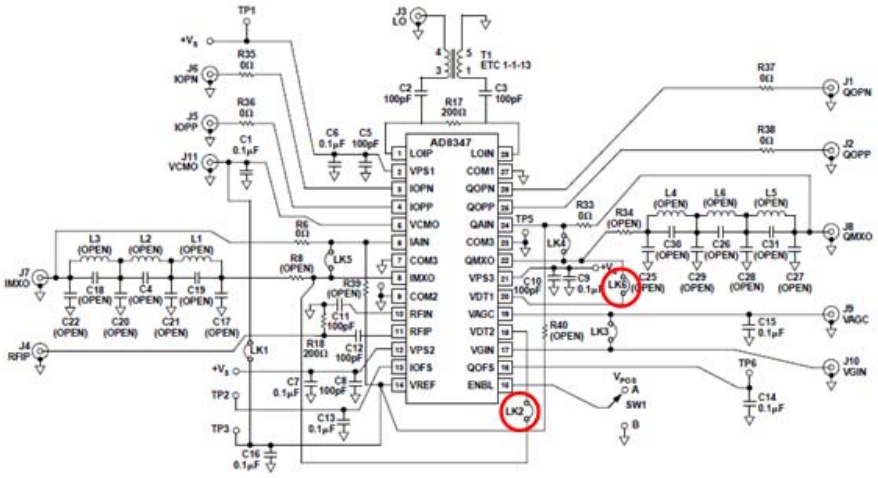

Figure 29. AD8347 Evaluation Board Schematic (From: [21]).

As for the VGIN mode configuration, some steps such as pulling the jumpers at LK2, LK3, and LK6 must be configured as shown in Figure 30.

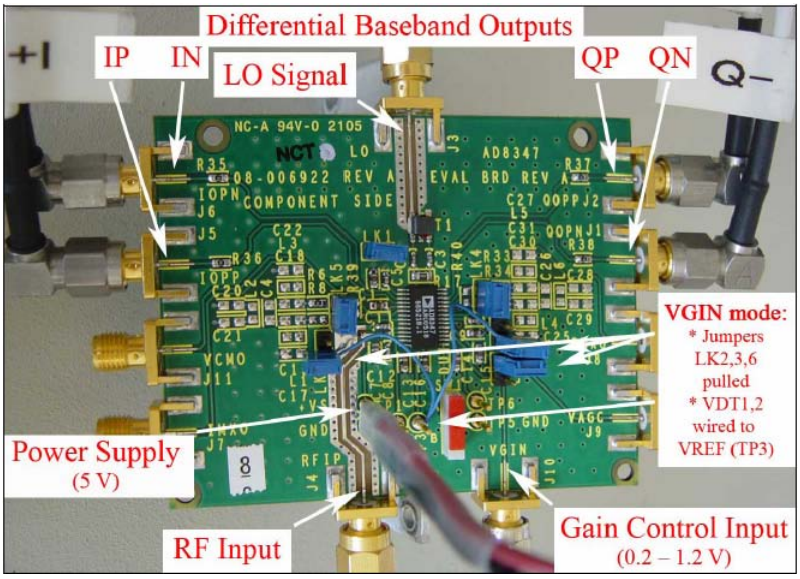

Figure 30. AD8347 Evaluation Board Wiring Connections and VGIN mode Setting (From: [18]).

The AGC mode was experimentally proven in [3] to have a wider dynamic range (of at least 25 dB) than that of VGIN mode. Thus, AGC mode is the preferred mode of

operation for most applications. The AGC mode measurement results extracted from [3] illustrated linearity for RFIN values between -36 dBm down to -61 dBm as shown in Table 2.

Board	Function	LO in [dBm]	RF in [dBm]	Circle radius [V]	I offset [V]	Q offset [V]	Circle
14	AGC	-11	-33	0.062	-0.0665	0.0421	Almost
14	AGC	-10	-36	0.053	-0.0684	0.0449	Yes
14	AGC	-11	-37	0.05	-0.067	0.0451	Yes
14	AGC	-11	-41	0.032	-0.0694	0.0447	Yes
14	AGC	-10	-51	0.012	-0.0691	0.0445	Yes
14	AGC	-10	-61	0.01	-0.0686	0.0443	Yes
14	AGC	-11	-63	0.005	-0.0696	0.0444	Yes
15	AGC	-11	-33	0.075	-0.0157	0.0219	Almost
15	AGC	-10	-36	0.055	-0.0232	0.0287	Yes
15	AGC	-10	-40	0.028	-0.0217	0.0304	Yes
15	AGC	-10	-50	0.015	-0.0219	0.0303	Yes
15	AGC	-11	-54	0.011	-0.0212	0.0301	Yes
15	AGC	-11	-57	0.011	-0.0211	0.0301	Yes
15	AGC	-11	-60	0.01	-0.0209	0.0296	Yes

Table 2. AGC Mode Linearity Measurement Result (From: [3]).

The measurement results also proved that the offset values for the RFIN signal circles are quite similar over the entire dynamic range of at least 25 dB. This means that DC offset calibration is only needed once per demodulator card [3].

In [18], the DC offsets of ten demodulators were measured to demonstrate that each demodulator card has its own unique value. Both actual and corrected I and Q response of the ten demodulator cards are shown in Figure 31.

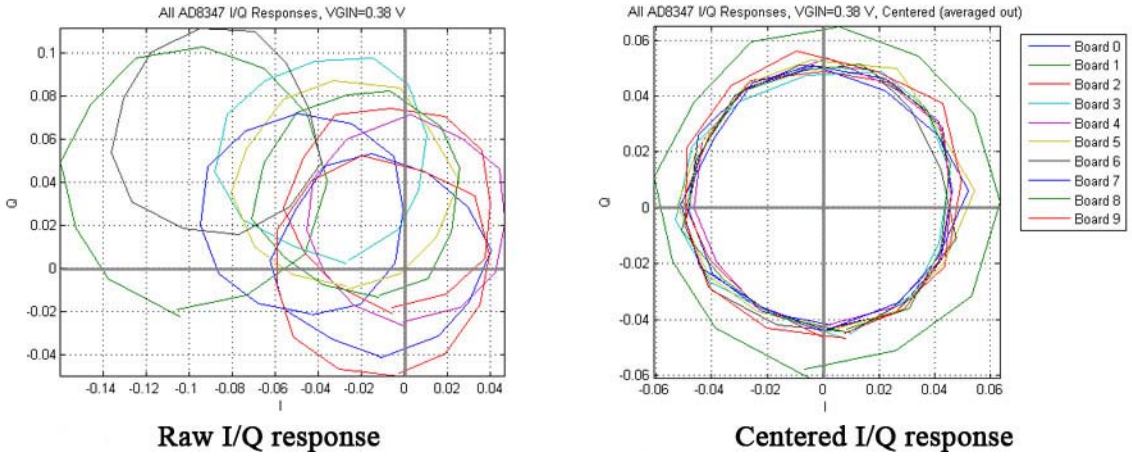

Figure 31. Plotted I and Q Circles of ten Demodulator cards (From: [18]).

According to [21], the specification of the AD8347 Demodulator Board RF Amplifier at P1 dB compression point is given as -30 dBm. P1 dB is the compression point as shown in Figure 32, after the linear region whereby the P_{in} or power input will only be amplified by a certain amount that is 1 dB less than the expected linear gain.

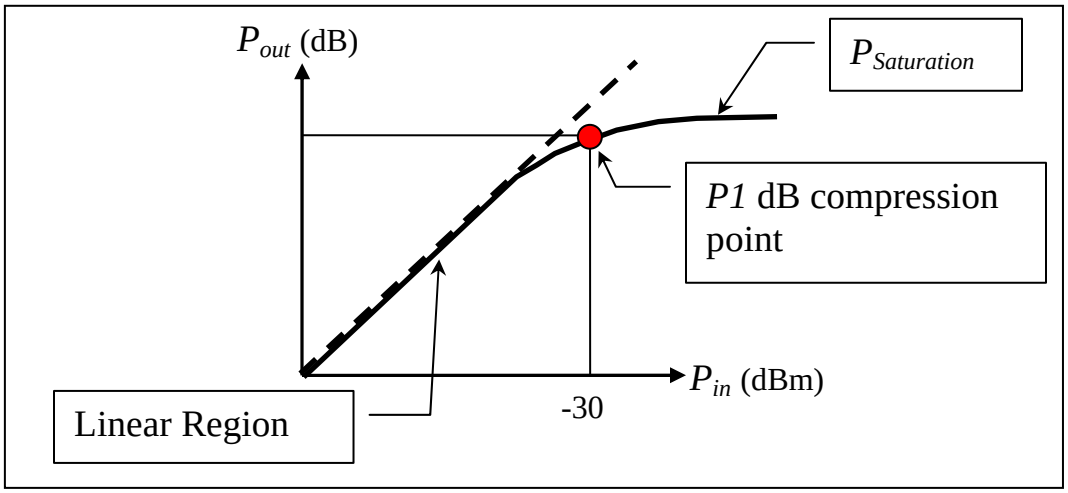

Figure 32. P1 dB Plot of AD8347 Demodulator Board RF Amplifier.

Thus P1 dB can be expressed in an equation form as:

$$P1dB_{output} = P1dB_{input} + (Gain - 1)\ dBm \quad (3.7)$$

The region after this P1 dB compression point is no longer linear and a rapid loss in gain is experienced. The component may fail if the input power continues to increase to the maximum limit [22]. Thus, it is advisable to operate the demodulator board less than the P1 dB compression point to have a linear gain power output.

An experiment was conducted to test the effects of non-linearity after P1 dB point. Calibration Test 1 was carried out using 39 dBm attenuated RF signal input to the demodulator board, and Calibration Test 2 was carried out using about 29 dBm attenuated RF signal input to the demodulator board. The result on the right hand side, with RF signal input set at about -29 dBm as shown, clearly illustrates the non-linearity effect whereby the I and Q circle is deformed and the calibrated I and Q offsets were erroneous.

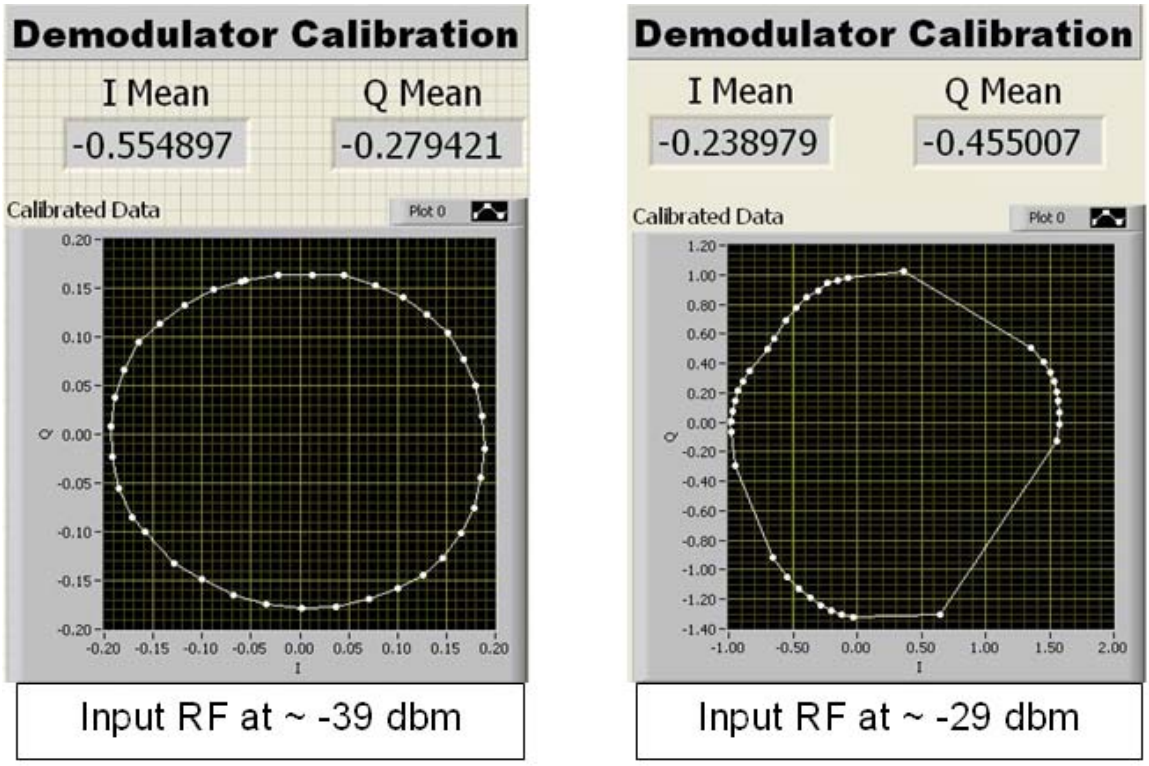

Figure 33. Effects of P1 dB Compression Point at -39 dBm and -29 dBm.

In conclusion, RF signal input to the AD8347 demodulator should be at least 6 dBm below the P1 dB compression point when designing the calibration station. In [3], this fact was further verified, demonstrating that the linear range for RFIN values was between -36 dBm down to -61 dBm.

3. Bamp Board

The function of the baseband differential instrumentation amplifier (Bamp) shown in Figure 34 is to convert the four differential output control signals (IP, IN, QP and QN) from the AD8347 direct conversion quadrature demodulator board into two I and Q signals.

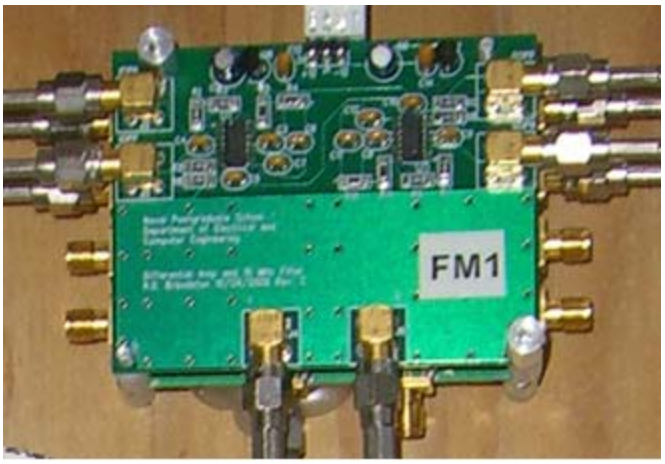

Figure 34. Bamp Board.

The Bamp board was specially designed and built by Robert Broadston, NPS Microwave Lab Director, to eliminate the need for costly and complex equipment to perform the similar task.

4. Signal Generator – LO signal

The function of the signal generator is to generate an LO signal for both the AD8346 modulator board and AD8347 demodulator via a power splitter. The Vaunix Technology Lab Brick LSG–402 signal generator, shown in Figure 35, was used as the signal source, primarily due to its small size and portability, making it easy to integrate into the overall calibration station.

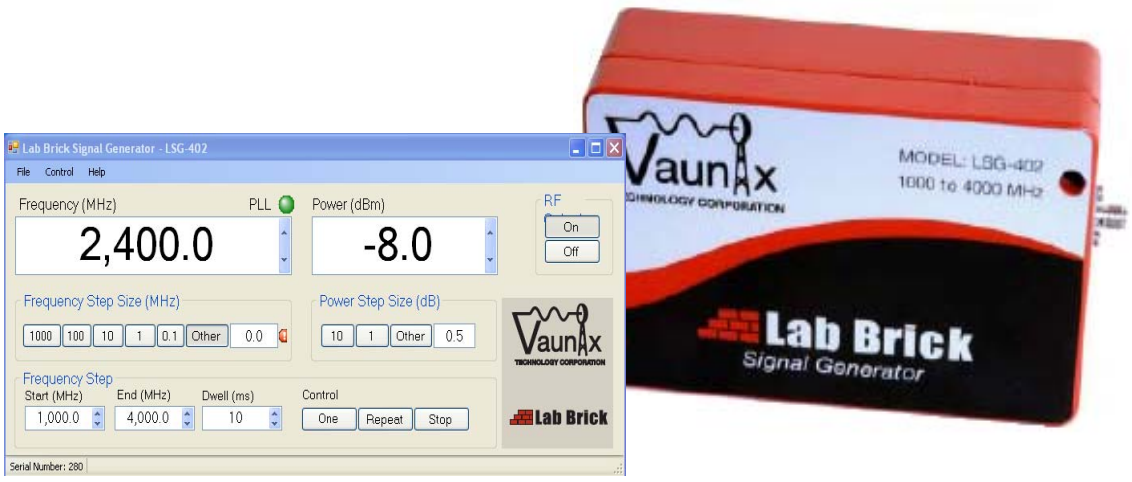

Figure 35. Lab Brick LSG-402 (After: [23])**.**

The Lab Brick LSG-402 signal generator is connected to the central controller via a USB port and can easily be controlled using a graphical user interface (GUI) for adjusting the frequency and power settings. The LO signal level settings are 2.4 GHz as the carrier frequency and -4.5 dB output power, taking into consideration the acceptable frequency range and dynamic range of both modulator and demodulator boards.

The LO signal level is quite stable and is within acceptable range needed for the calibration setup. According to [23], the non-harmonic spurious noise is typically at -80 dBc as shown in Figure 36.

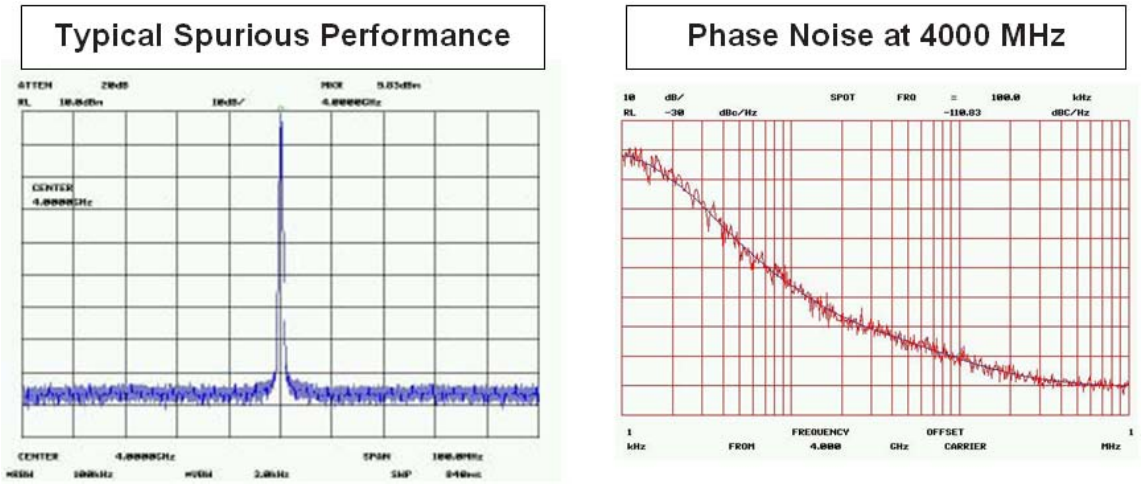

Figure 36. Performance Measurement of the Generated Signal (From: [23]).

5. Power Divider

The function of the power divider (shown in Figure 37) is to divide the LO signal generated by the signal generator into two and feed them into individual LO ports of the modulator and demodulator boards.

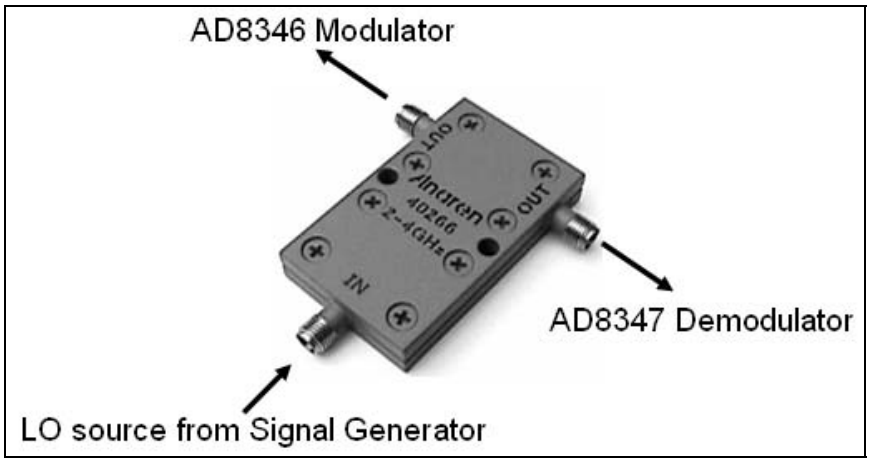

Figure 37. Anaren 40266 Power Splitter (After: [24]).

The power divider used for this application is 40266 power divider manufactured by Anaren. This power divider is robust for its class as it is manufactured to military-grade standard. The specifications of the power splitter are shown in Table 3 [25].

Specification:	Value
Frequency Range	2 – 4 GHz
Maximum Insertion Loss	0.3 dB
Maximum VSWR	1.3 SWR

Table 3. Anaren 40266 Power Divider Specification.

6. Power Supply

The function of the power supply (shown Figure 38) is to supply DC regulated power to the AD8346 modulator board and AD5347 demodulator board. The AC-DC regulated power supply was used due to its small size and acceptable specifications, such as DC output current and voltage.

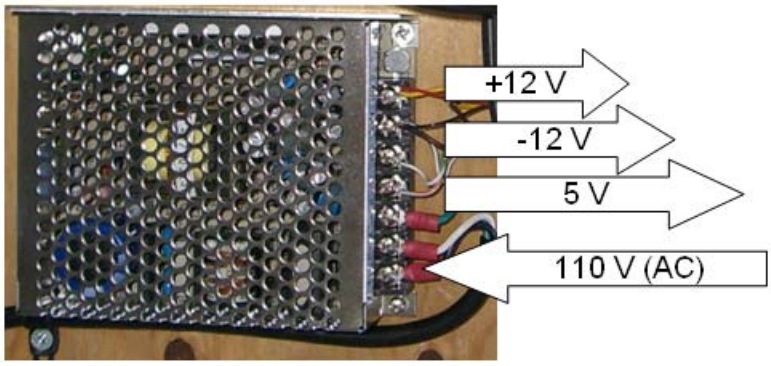

Figure 38. Regulated Power Supply.

The required regulated power to the various boards is shown in Table 1.

Equipment	Voltage	Current
Modulator Board	2.7 ~ 5.5 V	35 ~ 55 mA
Demodulator Board	2.7 ~ 5.5 V	48 ~ 80 mA
Bamp Board	+12 V	100 mA
	-12 V	100 mA

Table 4. Power Supply Specifications of Various Boards.

Three ferrite choke cores were used on the power cables to the modulator, demodulator and Bamp board respectively as shown in Figure 39.

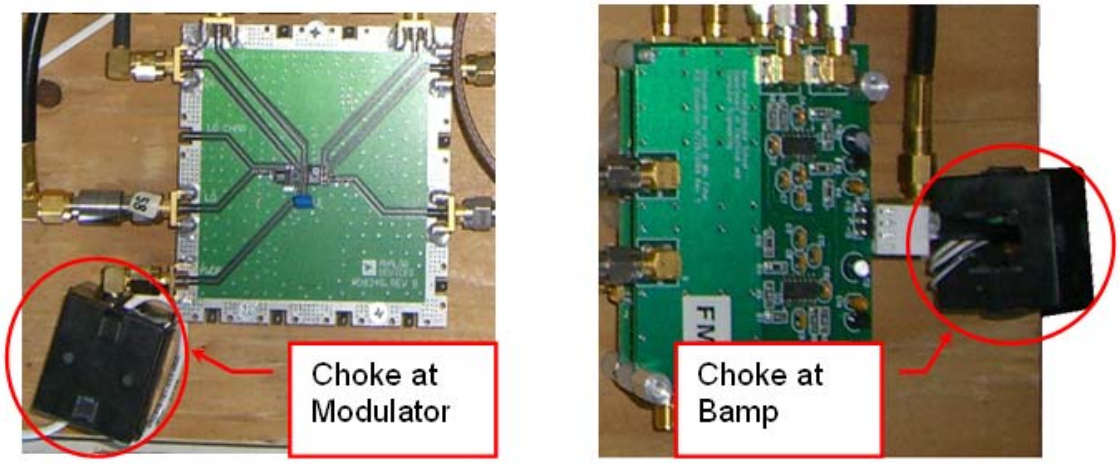

Figure 39. Ferrite Choke Core at Modulator and Bamp Board.

The chokes cut down on possible RFI (radio frequency interference) at high frequencies during calibration. The RFI signals are converted into heat in the choke core instead of radiating into the boards.

7. Attenuator

The functions of the attenuator is to attenuate the input signal to meet certain specifications of the various boards for LO signal input. Two attenuators labeled as Attenuator 1 and Attenuator 2 are necessary, as shown in Figure 40, for the calibration station design.

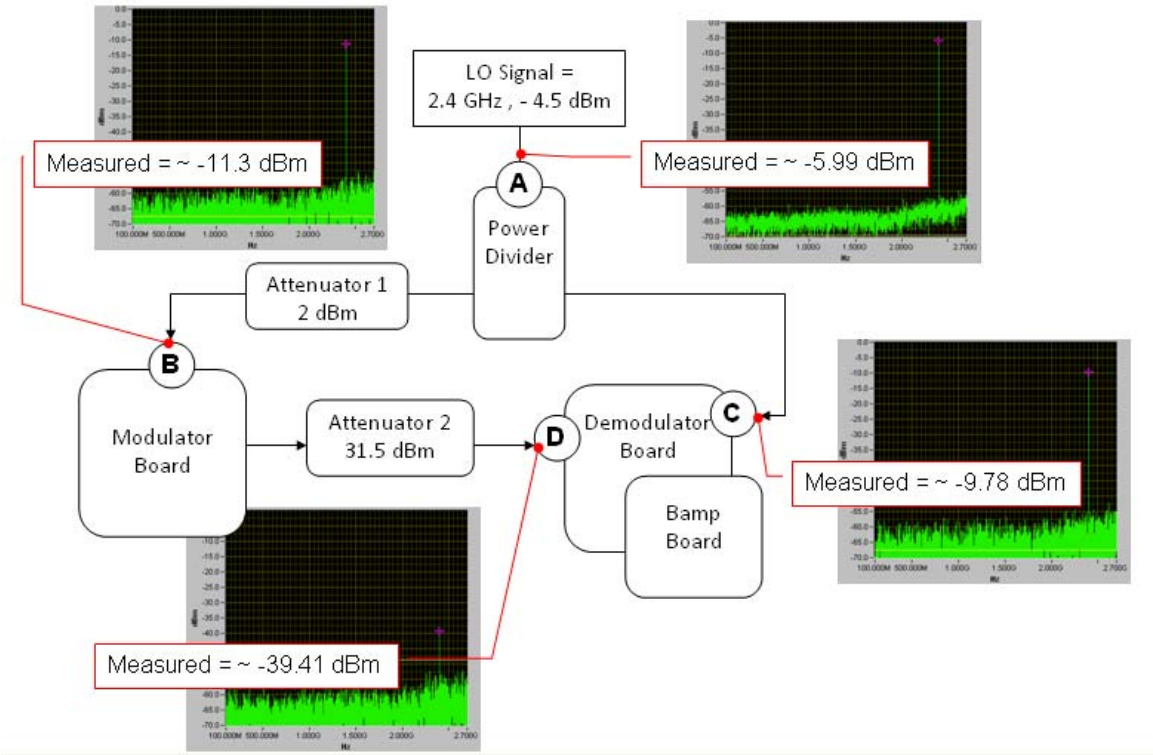

Figure 40. Attenuation Measurement.

The cable between the spectrum analyzer and point of measurement has a measured attenuation of about 1.5 dB as shown in Figure 41. Thus, it is necessary to calculate the actual power at each point, taking into consideration the attenuation of the cable. Thus, the recalculated values are shown in Table 5.

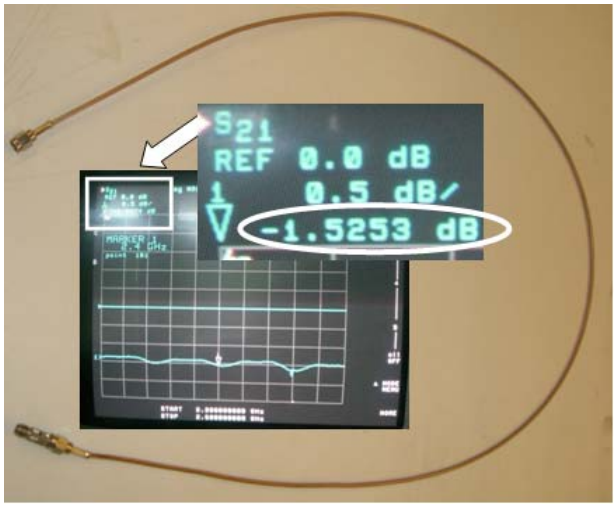

Figure 41. Cable Attenuation Measurement.

Measured Point	Description	Measured Value (dBm)	Calculated Actual Value (dBm)	Specification Requirement (dBm)
A	LO Source Signal	- 5.99	- 4.49	-4.5
B	LO signal to Modulator	-11.3	- 9.8	-10 (typical for AD8346)
C	LO signal to demodulator	- 9.78	- 8.28	-8 (typical for AD8347)
D	RF signal to Demodulator	-39.41	- 37.91	> - 30 (P1 dB for AD8347)

Table 5. Actual Measurement and Specification Requirement.

A 2 dB attenuator is needed at the modulator as the LO source is shared between demodulator and modulator with different LO signal requirements (typical) at -8 dBm and -10 dBm respectively. With the demodulator signal set as reference, the rest of the LO source setting and modulator LO input are tuned to this reference, such as LO source being set at -4.5 dBm.

At point A in Figure 40, the measured LO source signal of -4.9 dBm to the power divider is within requirement of -4.5 dBm. Thus, there will be -7.5 dBm supplied to the AD8346 modulator board and AD8347 demodulator board after the power divider.

At point B, the measured supply LO signal is -9.8 dBm after a 2 dB attenuator is added to meet the typical specification of AD8346 modulator board at -10 dBm. For optimum performance of the system, this 2 dB attenuator was used, although it is still in the specification range of -12 dBm to -6 dBm without the 2 dB attenuator.

At point C, the measured supplied LO signal is -8.28 dBm, which meets the specification value of -8 dBm. Again it is recommended (more optimum) to operate the demodulator board at value at the center of the specification range, rather than at the extreme ends of the range (-10 dBm to 0 dBm).

At point D, the measured RF signal to the demodulator is -37.91 dBm, which is below the P1 dB compression point of -30 dBm. The ill effects of operating beyond compression point had been discussed in Section 2.

C. DESCRIPTION OF SIGNAL PROCESSING COMPONENTS

1. NI PXI-1044

The National Instrument (NI) PXI platform is designed for measurement and automation applications. The PXI-1044 is personal computer (PC) chassis that houses the controller and several PCI extensions for instrumentation (PXI) cards is shown in Figure 42.

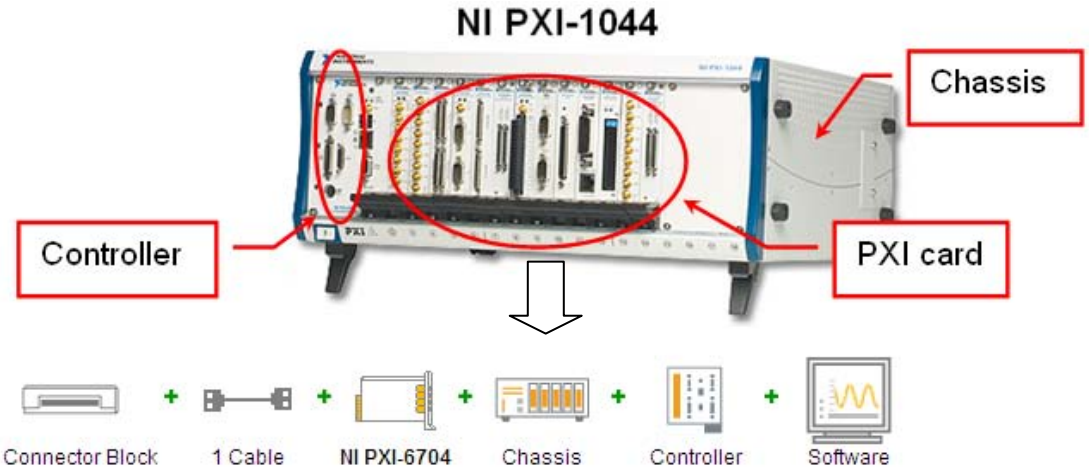

Figure 42. NI PXI 1044 (From: [26]).

It has 14 slots that accept both CompactPCI and PXI modules. For current calibration station application, two PXI cards are needed, namely a PXI-6704 for digital-to-analog conversion purposes and a PXI-5112 card for measurement of the I and Q signals. With the controller, it is able run a Windows-based program, such as NI LabVIEW, that controls both PXI cards.

2. NI PXI-6704

This PXI-6704 card (shown in Figure 43) is a digital-to-analog convertor (DAC) that converts digital signals into analog form. It is integrated onto the PXI-1044 chassis as part of the overall hardware that supports the LabVIEW calibration program.

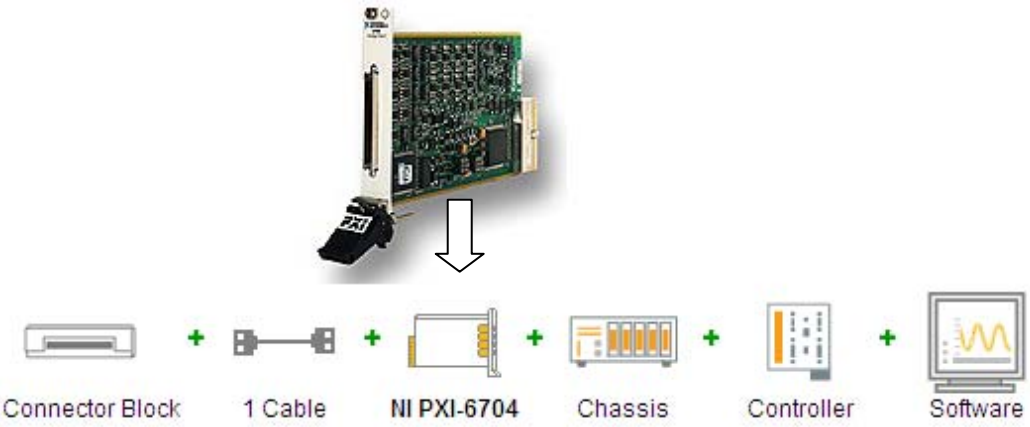

Figure 43. NI PXI 6704 Interfaces (After: [27]).

It converts the four digital differential control signals (IP, IN, QP, QN) after generation by the LabVIEW calibration software into analog forms. As explained in Section 1, these four converted analog differential control signals are needed as the baseband signals for phase shifting and modulation purposes on the AD8346 modulator board.

3. NI TBX 68

As seen in Figure 44, TBX 68 is a connector block with 68 screw terminals that connects field I/O signals to the 68-pin data acquisition output port of the PXI 6708 via a SCSI cable.

Figure 44. NI TBX 68 (After: [28]).

4. NI PXI-5112

The function of the PXI-5112 is to convert the I and Q analog signals from AD8347 demodulator board into digital format for post processing, such as calculation of the DC offset and plotting of the I and Q circle. It is a high-speed 100 MHz digitizer that uses 8-bit analog-to-digital converters and low-noise variable-gain amplifiers as shown in Figure 45.

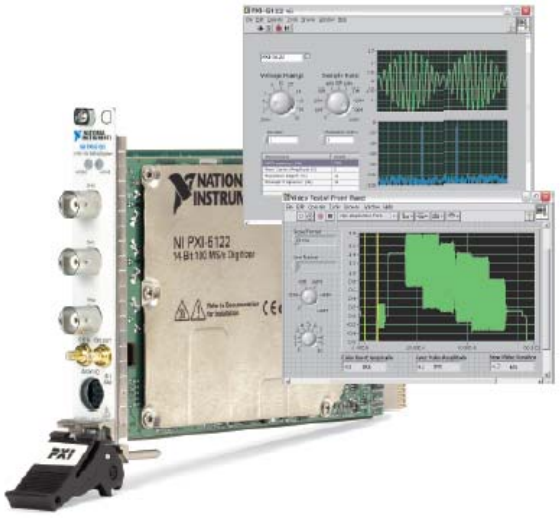

Figure 45. NI PXI 5112 Digitizer (From: [29]).

5. LabVIEW Calibration Program

The LabVIEW calibration program consists of the front panel, which is the graphical user interface (GUI) and runs on top of a back end program (i.e., the LabVIEW block diagram). The front panel GUI is illustrated in Figure 46. It is an important interface or link between the user and the calibration sequence control. It allows the user to control the calibration parameters such as I and Q amplitude, phase shift increment, transmit/receive (Tx/Rx) delay, phase shifting delay, and LO power level and frequency. Some of these parameters are highlighted in the figure.

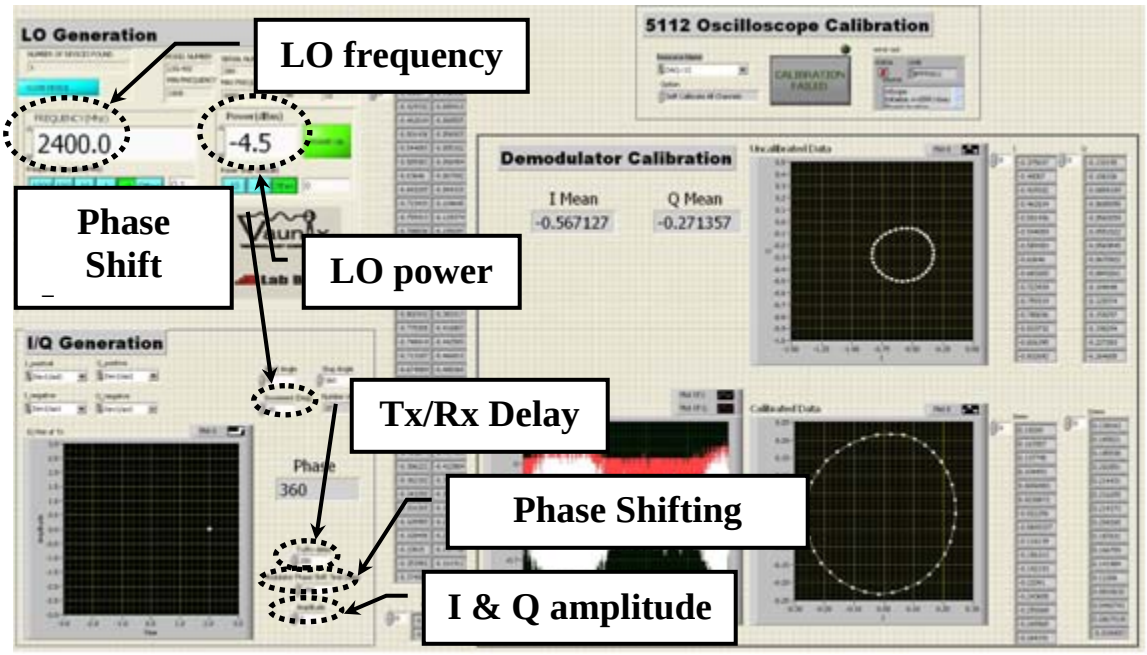

Figure 46. Calibration Front Panel GUI.

The back end LabVIEW calibration program can be classified into four main functions: (a) phase shifting/modulation, (b) demodulator calibration, (c) PXI 5112 calibration, and (d) LO generation as shown in Figure 47. The following sections will further elaborate these four main functions.

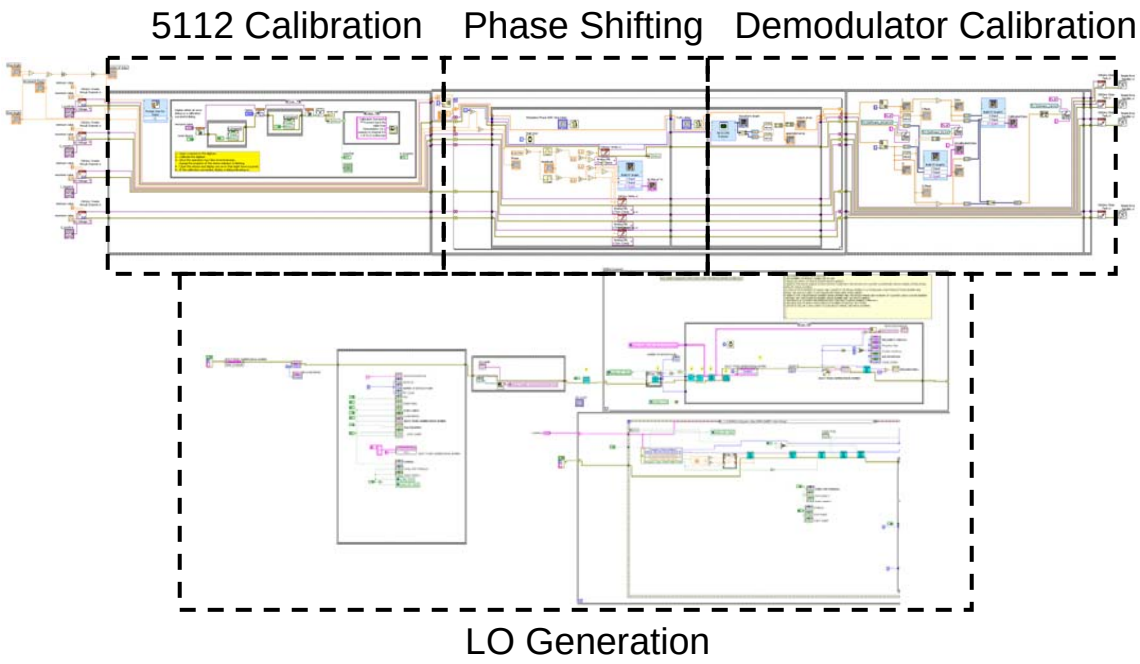

Figure 47. LabVIEW Calibration Program Block Diagram.

(a) Phase Shifting/Modulation Function

This function, highlighted in Figure 48, is used to generate the four differential control signals (IP, IN, QP, IN) as the baseband signal for phase shifting and modulation purposes.

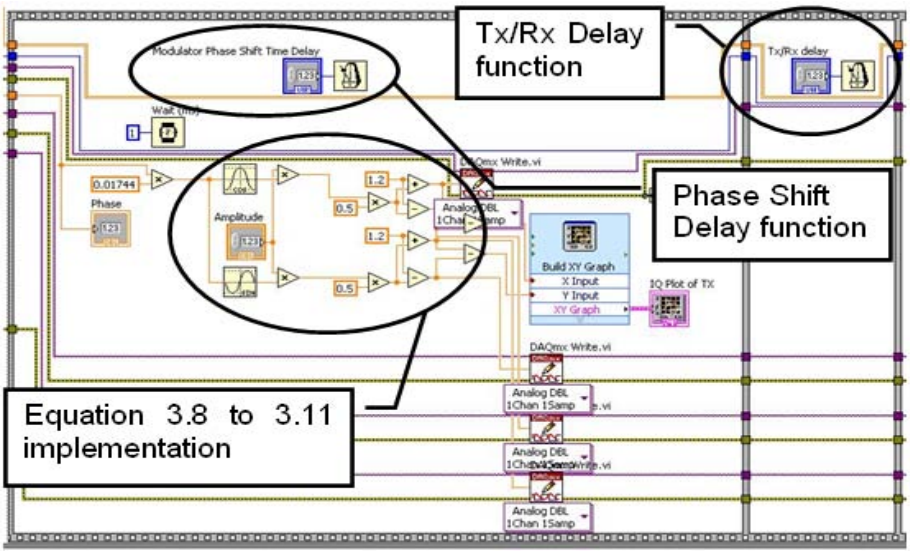

Figure 48. Phase Shifting/ Modulation Function.

The generation of these control signals is based on implementation of Equations (3.3) to (3.6). The program will cycle through from 0^0 to 360^0 phase shift at 10^0 steps (the step size can be changed but the default value is 10^0).

As shown in Figure 48, there are two delay functions in the system. One is the time interval between every phase shift, known as phase shift delay function. The other is the time delay before sampling by the PXI-5112 digitizer. The phase shift delay function is needed to stabilize the system due to some transients when shifting from one phase to the other as shown in Figure 49. In the figure, the transmitted I and Q voltages are changed and then held constant. However, the received I and Q values continue to change during the first few samples.

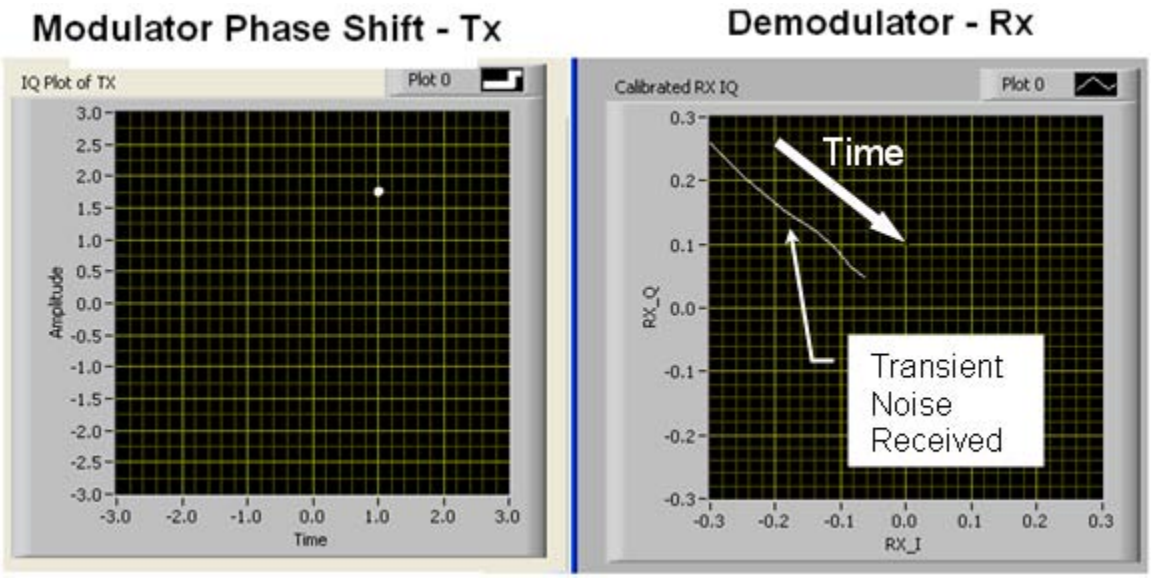

Figure 49. Received Signal affected by Transient Response.

A transmit/receive (Tx/Rx) delay function of 250 ms (default setting) that acts like a time gate was added in between the modulator transmit sequence and demodulator receive sequence to prevent sampling data with transient noise. The I and Q circle can be distorted at few points without any delay filtering between phase shifts as shown in Figure 50. This delay can be altered via the GUI prior to the start of each calibration cycle.

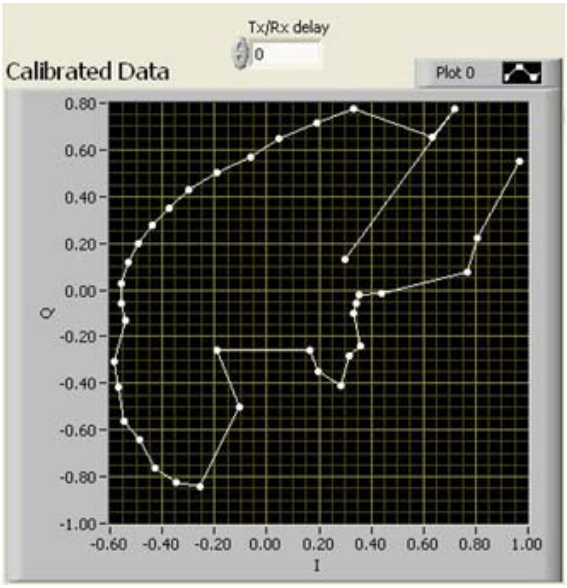

Figure 50. I and Q Circle Distortion during Phase Shift without Delay Filtering.

Next, the LabVIEW digitally generated control signals are converted into analog format via PXI 6704 DAC before finally reaching the AD8346 modulator board. The I and Q differential input values are set at default 2.0 V unless altered by the user via the amplitude setting on the GUI prior to start of calibration as shown in Figure 51.

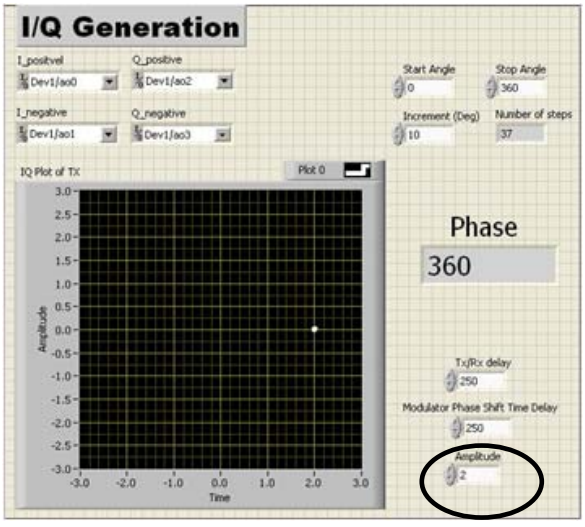

Figure 51. User Input - Amplitude Setting.

(b) Demodulator Calibration Function

This function, shown expanded in Figure 52, is primarily used to post process the measured I and Q demodulated signal from the AD8347 demodulator board via the PXI 5112 digitizer (ADC).

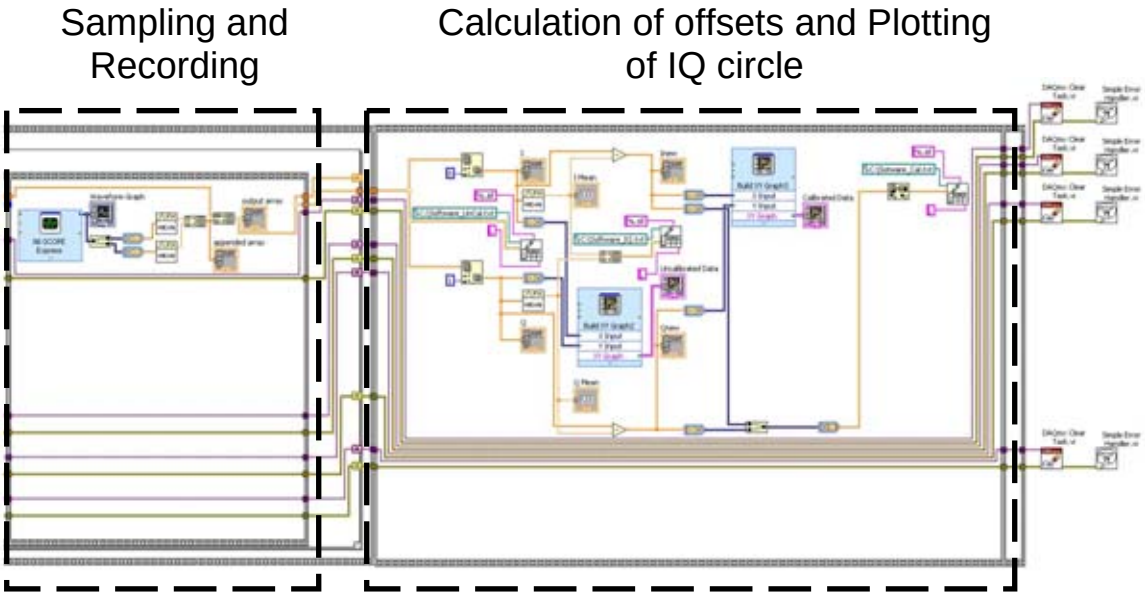

Figure 52 LabVIEW Demodulator Calibration Function.

Post processing includes recording of the uncalibrated (raw) I and Q measured values after each 10^0 phase shift of the modulator, calculating the mean value of these uncalibrated/raw values and, lastly, calculating the I and Q offset from the zero reference. The program records 10,000 samples at each phase shift and calculates the mean I and Q values, which are then saved. For 10^0 steps, total set of 37 I and Q values will be recorded starting from phase 0^0 to 360^0. Both uncalibrated and calibrated plots of the I and Q circle are shown on the calibration GUI at the conclusion of calibration.

(c) PXI 5112 Calibration Function

The calibration function, as its name suggests, calibrates the PXI 5112 digitizer. This is necessary prior to the start of each calibration process to achieve a consistent and error-free demodulator calibration result. The LabVIEW library program shown in Figure 53, known as “niScope EX Calibrate.VI”, runs this calibration. It was downloaded from

National Instruments (NI) and integrated with the overall calibration program for ease of use.

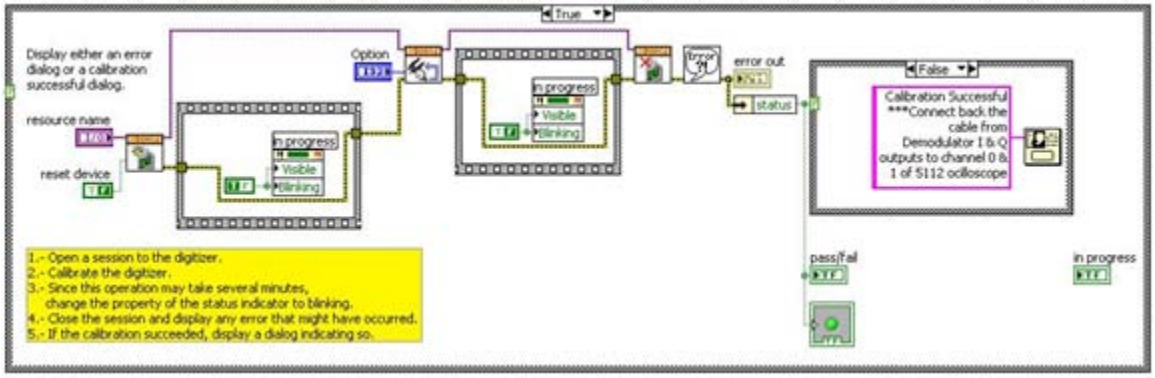

Figure 53 LabVIEW PXI 5112 Calibration.

The physical process of the PXI 5112 calibration involves connecting two shorting plugs, as shown in Figure 54, at each end of both incoming channels of the PXI 5112. The purpose of these two shorting plugs is to ground any possible floating signal for better calibration accuracy.

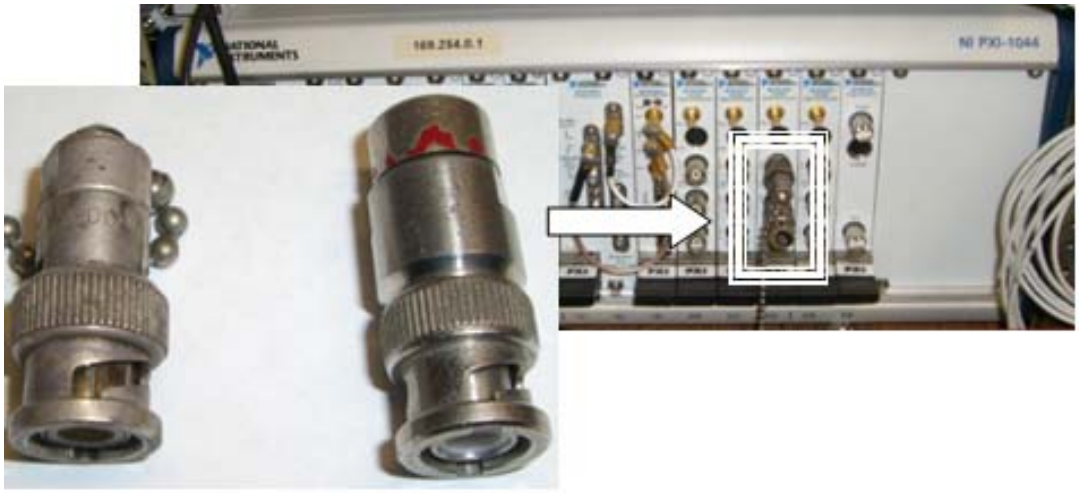

Figure 54. Calibration Shorting Plugs.

(d) LO Generation Function

This function was used to control the LabBrick signal generator application for transmitting an LO signal to both the AD8346 modulator and AD8347 demodulator cards. The LabVIEW program, shown in Figure 55, known as “Vaunix Generator.VI”,

controls the signal generator. It was downloaded from the LabBrick manufacturer and integrated with the overall calibration program for ease of use in single control panel.

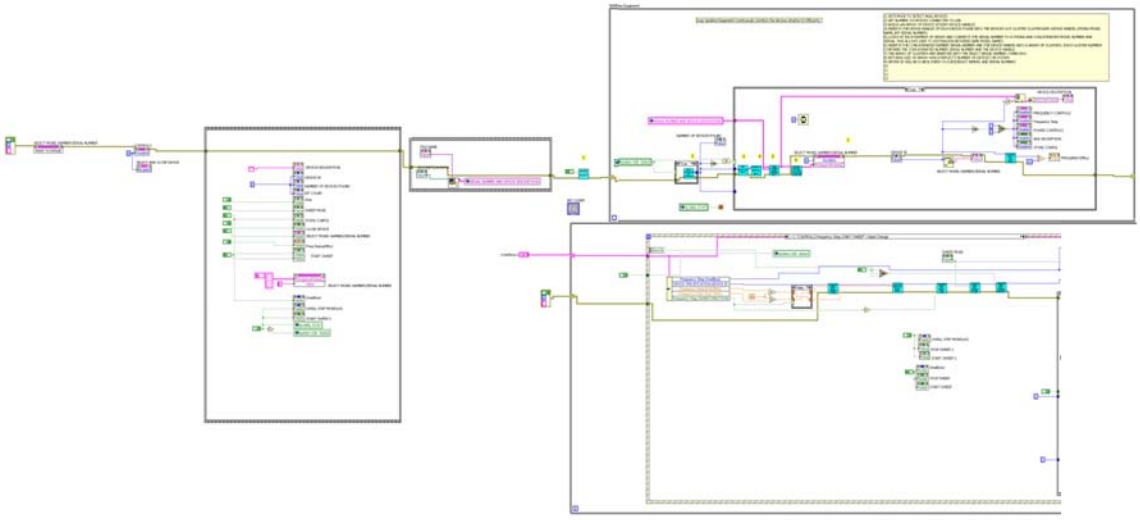

Figure 55. LabVIEW for LabBrick Signal Generator.

D. SUMMARY

In this chapter, the hardware and software system used for the implementation of the automated calibration station were described. The functional block diagram illustrates the individual sub-systems used for the final integration of the calibration station. The functional and specification aspect of each system were also elaborated. In the next chapter, calibration procedures and the validation tests will be discussed.

IV. IMPLEMENTATION AND VERIFICATION

This chapter describes the calibration procedures for the new automated calibration station and the optimized parameter settings. Further validation tests were carried out to characterize the calibration station and justify the recommended optimized parameter settings.

A. CALIBRATION DEMONSTRATION

1. Setup

The hardware and software components as explained in Chapter III were integrated together as a full automated calibration station for AD8347 demodulator boards as shown in Figure 56.

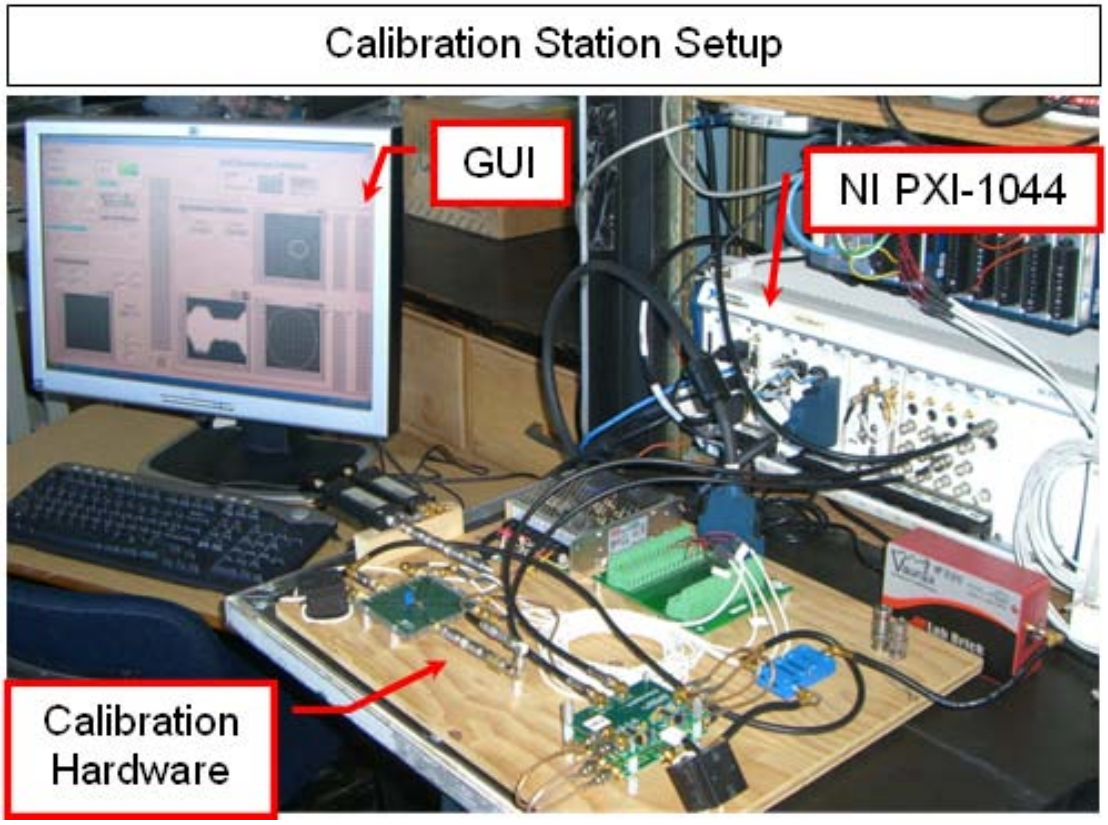

Figure 56. Calibration Station Setup for AD8347 Demodulator Board.

The setup consists of the calibration hardware, NI PXI-1044 and GUI. Most of the calibration hardware such as modulator board, power supply, TBX 68 connector board, power divider and demodulator board, are physically mounted onto test board. This test board allows for ease of portability and use during field testing when lab-based bench testing is not possible. The NI PXI-1044 is the processing mechanism for the calibration station, as it carried out tasks such as generating the four analog differential control signals (IP, IN, QP, QN), post processing of the received I and Q data, and allowing user interface via GUI. The GUI of the calibration system allows users to interact with the calibration station for operations, such as controlling the amplitude of I and Q signals and displaying the calibrated DC offsets results. The GUI was designed to be user friendly and includes guidance for each calibration step.

2. Calibration Procedures and Results

The following sections delineate the calibration procedures starting from step 1 to step 3 as shown in Figure 57.

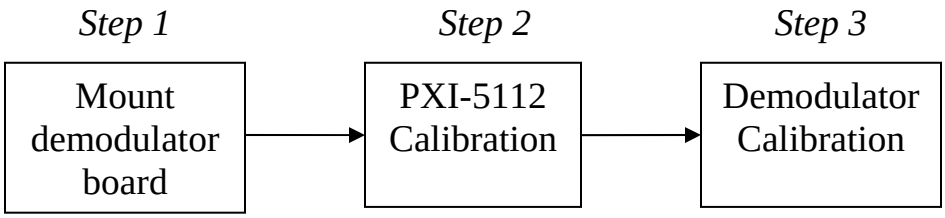

Figure 57. Block Diagram of Calibration Step.

(a) Step 1: Mounting of demodulator board

The user is required to mount the uncalibrated demodulator board along with its Bamp board onto the test board jig (a demodulator and its Bamp board must be calibrated together). This is done in a simple step of unscrewing the four mounting screws and placing them onto the test board jig as shown in Figure 58.

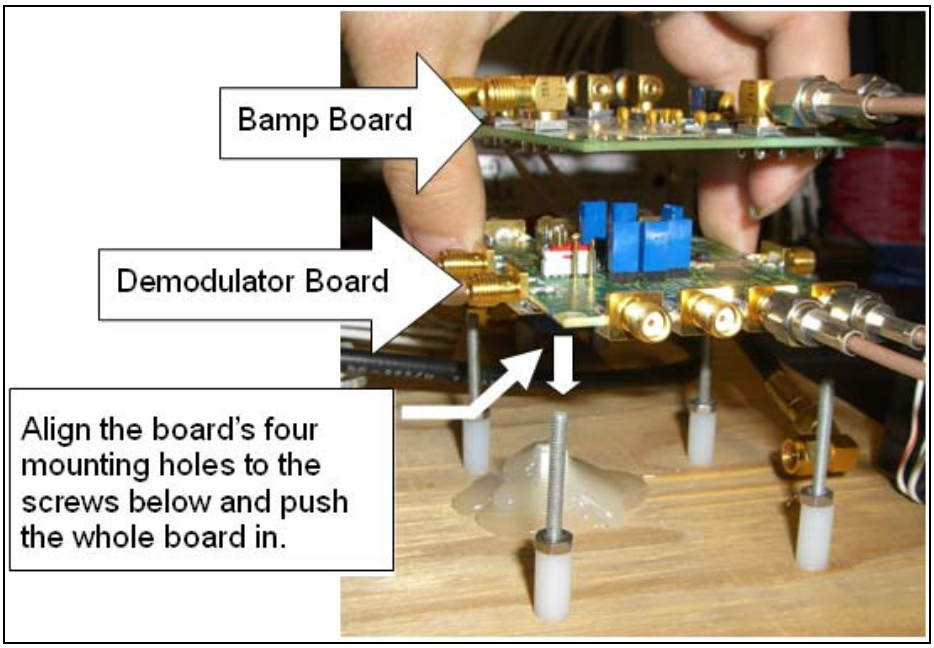

Figure 58. Mounting the Uncalibrated Demodulator Board.

Next, connect the five cables, as shown Figure 59, to the demodulator and Bamp boards and the physical setup is done.

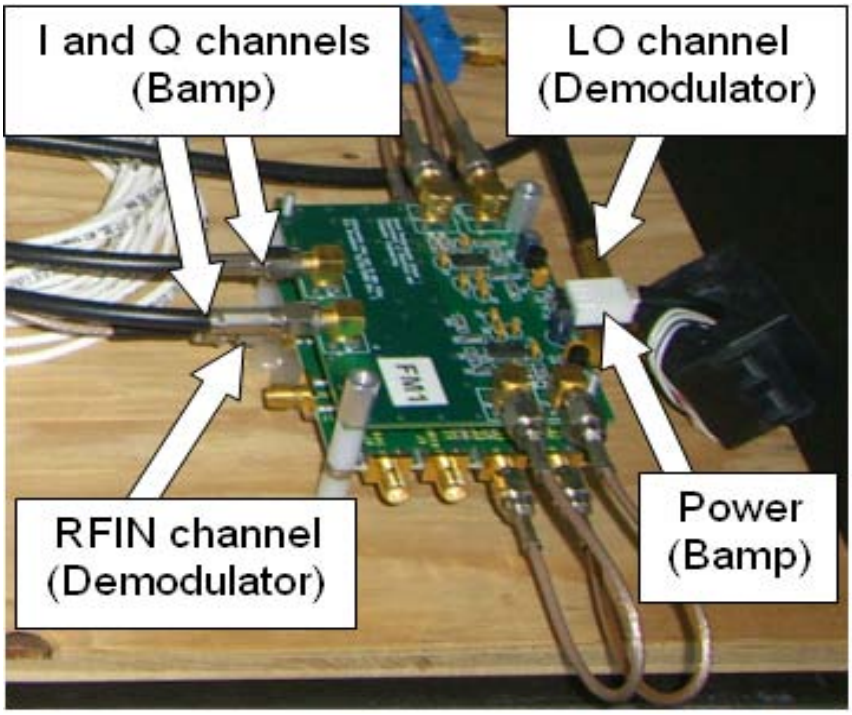

Figure 59. Connecting the cables to Demodulator and Bamp Board.

(b) Step 2: PXI 5112 digitizer calibration

The user must ensure that the LO signal is set at 2.4 GHz and -4.5 dBm on the GUI panel before running the LabVIEW calibration program. The program starts with an option to choose either PXI 5112 calibration first or go directly to the demodulator calibration as shown in Figure 60, as PXI 5112 digitizer calibration is required only at the initial power up of the equipment.

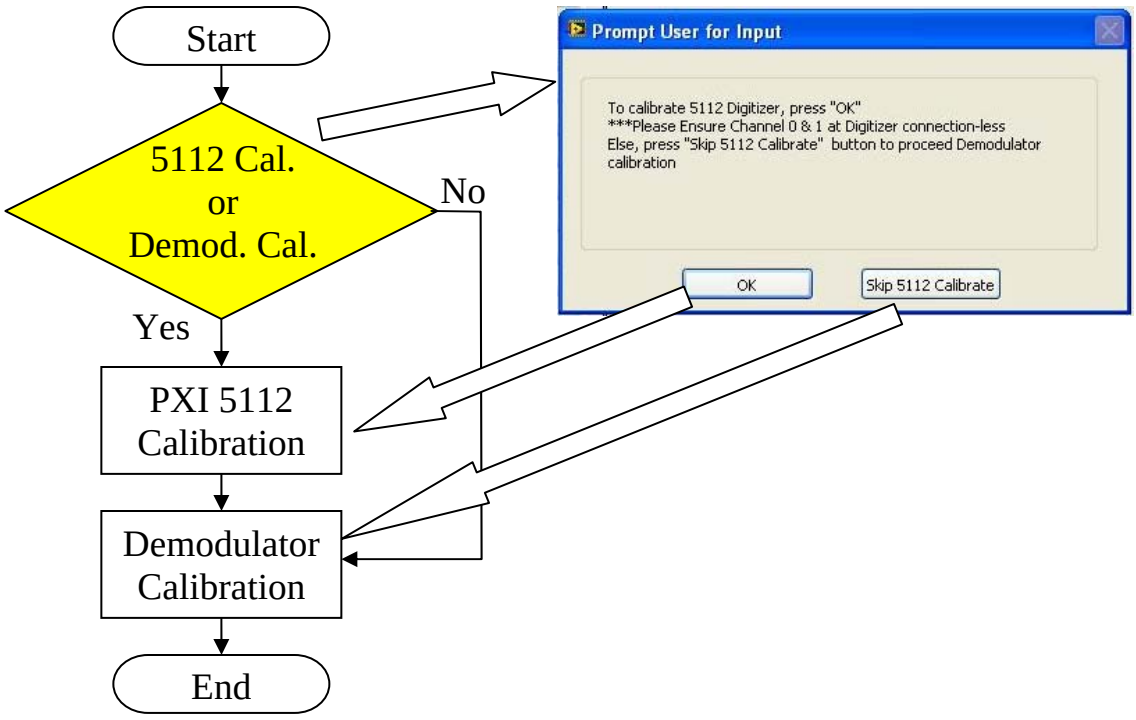

Figure 60. Flow Chart of Calibration Process.

If PXI 5112 digitizer calibration option is selected, the user is required connect the shorting plugs prior to the start of calibration. Next, the program will proceed with the start of the 5112 calibration, typically taking an estimated time of less than 70 seconds.

(c) Step 3: Demodulator Calibration

At the end of PXI 5112 digitizer calibration comes the final step of the process, which is the demodulator calibration. The program prompts the user to disconnect the shorting pins and reconnect the cables from the Bamp board (I and Q ports) to PXI 5112 (channel 0 and 1 ports) as shown in Figure 61.

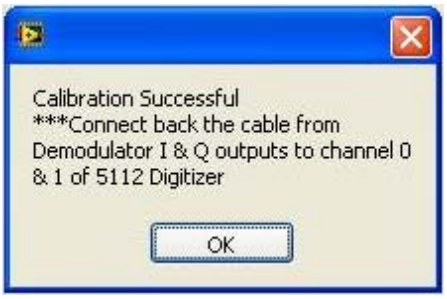

Figure 61. Prompt User to Disconnect the Shorting Pins.

Next, the program runs the phase shifting/modulation function to generate I and Q signal phases from 0^0 to 360^0 at a 10^0 step interval. Post processing calculation of the uncalibrated (raw) I and Q values is carried out, which generates I and Q offset values. Both uncalibrated and calibrated plots of the I and Q circle are generated as shown in Figure 62.

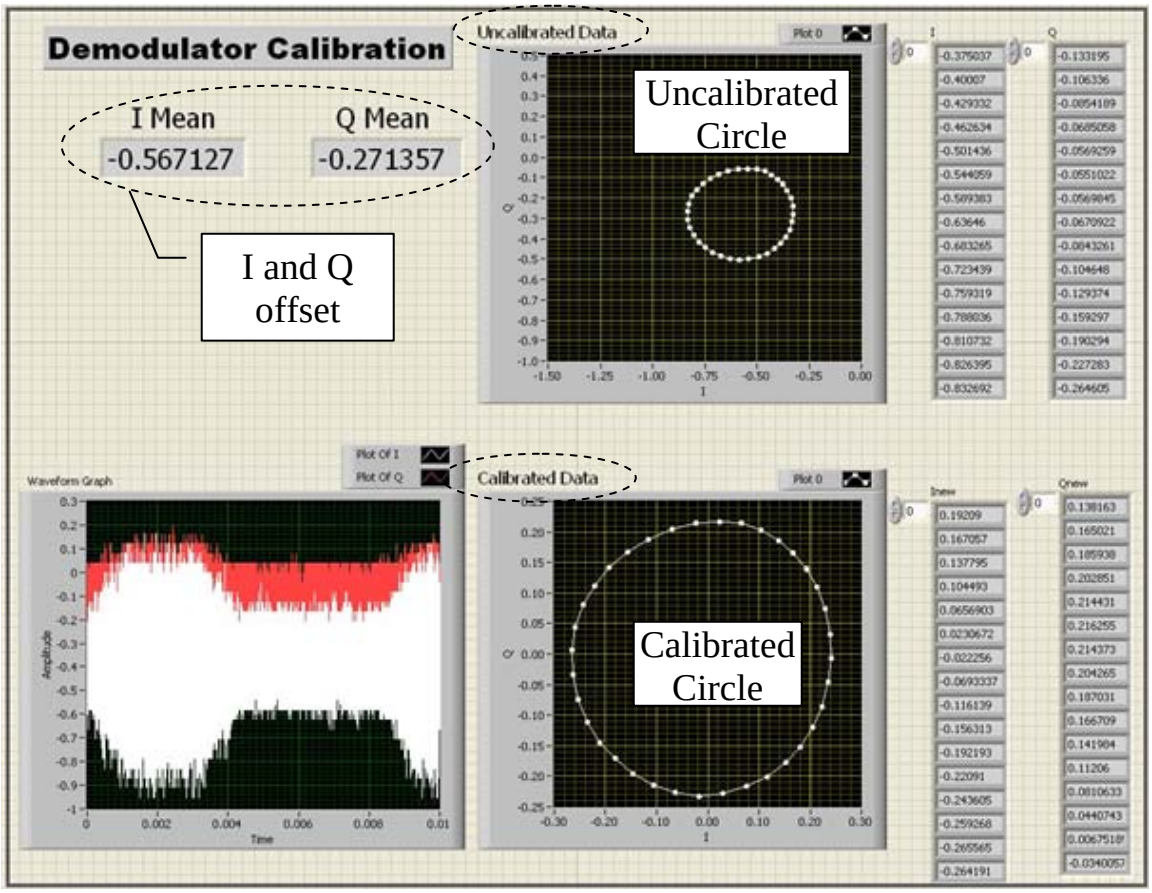

Figure 62. Calibration Results.

We can observe from Figure 63 that the uncalibrated IQ circle was at I and Q offset value calculated at -0.567127 and -0.271357. Thus, we can shift this uncalibrated IQ circle back to the center or origin with the offset values to form the new calibrated circle.

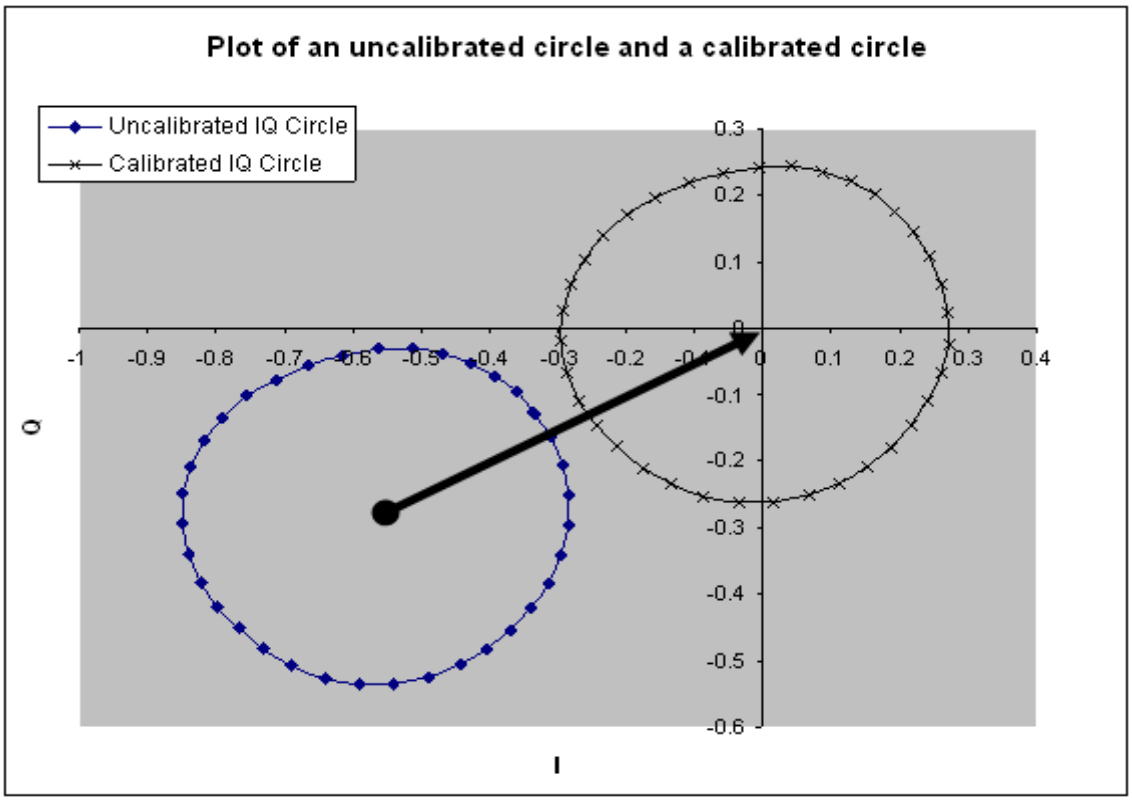

Figure 63. Plot of an Uncalibrated and Calibrated Circle.

B. VALIDATION

The test station validation is an important process as it helps to verify the new automated calibration station performance and accuracy. Validation of the automated calibration cannot be carried out by any theoretical calculations as each AD8347 demodulator board has its own unique DC offset values [18]. Thus the only possible solution is to compare station data to that collected with the old manual calibration method. Figure 64 shows the calibrated I and Q circles for both calibration stations for a set of measurements.

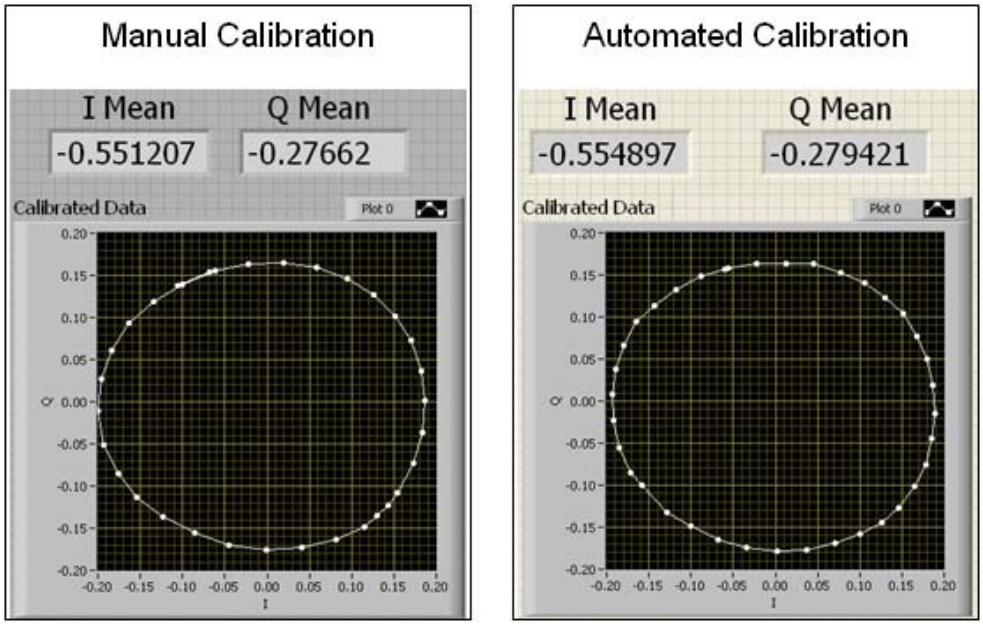

Figure 64. I and Q plots for Manual and Automated Calibration.

Five sets of measurements were taken with each calibration station. Their average measurements are tabulated in Table 6.

Manual Calibration		
Result #	I	Q
1	-0.551207	-0.27662
2	-0.559585	-0.268766
3	-0.559465	-0.269045
4	-0.554215	-0.270584
5	-0.554927	-0.266238
Average	-0.5558798	-0.2702506

Automated Calibration		
Result #	I	Q
1	-0.554897	-0.279421
2	-0.55421	-0.278733
3	-0.554375	-0.278534
4	-0.552272	-0.279499
5	-0.551437	-0.278824
Average	-0.5534382	-0.2790022

Table 6. Measurements of Manual and Automated Calibration.

For both calibration stations, the average measurements were very close. Thus, the difference is only 0.44 % for I values and 3.14 % for Q values. It can be observed that the automated calibration station is very accurate when compared against the manual calibration station and thus met the objectives of this thesis in terms of accuracy. An

equally important parameter is the time taken. The automated calibration duration was only 1/10 of the manual calibration duration and also eliminated the user's requirement of manually turning the phase shifter.

C. CHARACTERIZING THE PXI-5112 DIGITIZER

Subsequently, more tests were conducted to define the characteristics of the calibration station. These tests included studying the effects of using different PXI-5112 digitizer cards, to examine if measured I and Q values differ significantly from card to card and how significant this difference is, if any. This is important to know when the boards are used in a real system.

From the calculated average measurements of each card in Table 7, it can be observed that the difference between them is small; they are unchanged up to two decimal places. However, for some applications, it will be more accurate and advisable to use the same PXI 5112 card for calibration and keep it with the demodulator board in the system.

	Card 1		Card 2		Card 3		Card 4	
Result #	I	Q	I	Q	I	Q	I	Q
1	-0.5508	-0.2643	-0.5666	-0.2762	-0.5549	-0.2794	-0.5538	-0.2679
2	-0.5511	-0.2641	-0.5671	-0.2755	-0.5542	-0.2787	-0.5541	-0.267
3	-0.5504	-0.2639	-0.5667	-0.2761	-0.5544	-0.2785	-0.5531	-0.2669
4	-0.5509	-0.2647	-0.5667	-0.2766	-0.5523	-0.2795	-0.5533	-0.2677
5	-0.5513	-0.2638	-0.5661	-0.276	-0.5514	-0.2788	-0.5527	-0.2677
Average	-0.5509	-0.2642	-0.5667	-0.2761	-0.5534	-0.279	-0.5534	-0.2674

Table 7. Measurements Recorded Using Different PXI 5112 Card.

D. CHARACTERIZING THE DYNAMIC RANGE

The P1 dB, or compression point of the AD8347 demodulator board is given as -30 dBm [21], thus it is recommended to maintain the RFIN to the demodulator board

below the compression point. In [3], the recommendation was to operate the RFIN within the linear range, between -36 dBm and -62 dBm. However, there is a question of exactly how much the RFIN power should be provided during the calibration process within that linear range. Further measurements at various RFIN power levels were taken. To evaluate the accuracy of I and Q offset values and the shape of calibrated IQ plots, the recorded measurements are shown in Figure 65.

RFIN Power (dBm)	Calibrated (I) offset value (V)	Calibrated (Q) offset value (V)	Delta value for I	Delta value for Q
-30	-0.218236	-0.463582	0	0
-31	-0.286765	-0.455956	0.068529	0.007626
-32	-0.303553	-0.412658	0.016788	0.043298
-33	-0.362248	-0.366663	0.058695	0.045995
-34	-0.456685	-0.30418	0.094437	0.062483
-35	-0.54467	-0.285917	0.087985	0.018263
-36	-0.554883	-0.272792	0.010213	0.013125
-37	-0.55457	-0.272953	0.000313	0.000161
-37.5	-0.554463	-0.272852	0.000107	0.000101
-38	-0.553499	-0.272269	0.000964	0.000583
-39	-0.549439	-0.270374	0.00406	0.001895
-40	-0.544584	-0.269755	0.004855	0.000619
-41	-0.544053	-0.270193	0.000531	0.000438
-42	-0.543	-0.269646	0.001053	0.000547
-43	-0.541843	-0.271016	0.001157	0.00137

Figure 65. Measured of I and Q from RFIN = -30 dBm to -43 dBm.

A plot was generated to analyze the I and Q offset values at various power levels as shown in Figure 66.

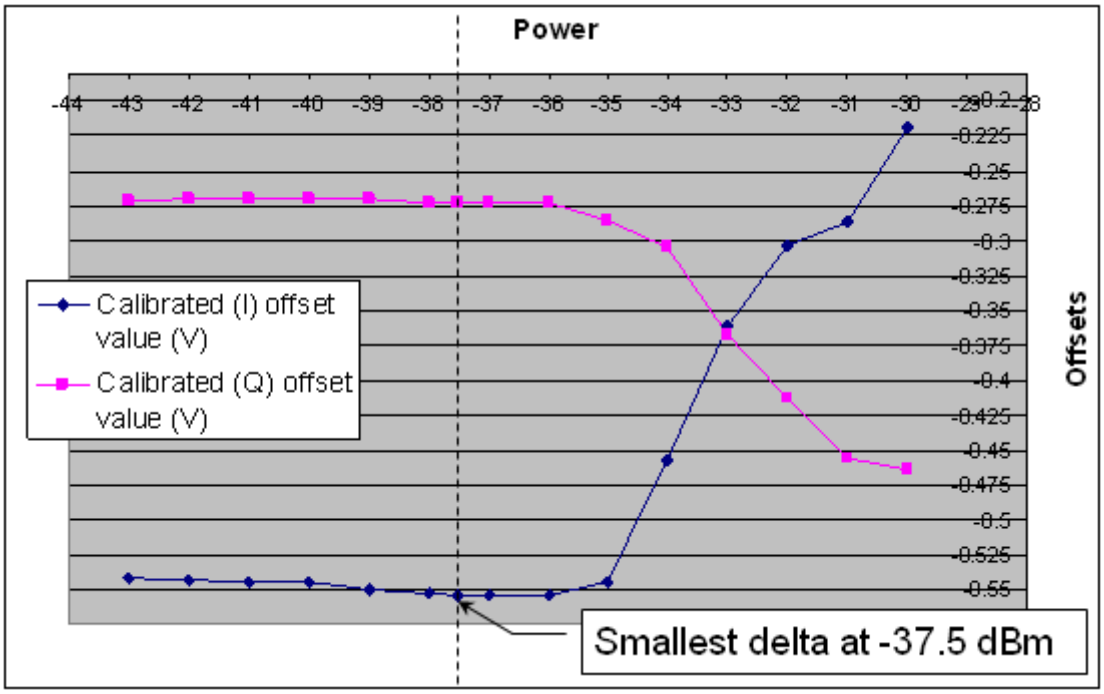

Figure 66. A plot of Power Level versus I and Q Offset values.

Starting in the non-linear region, for each power level, the I and Q offset values were measured. The delta for each power level is that level's offset values minus the previous ones. The highest delta is between -30 dBm to -36 dBm. In addition, I and Q circles formed in this range are distorted as shown in Figure 67. This is due to the region near the P1 dB, which is beginning to be non-linear as shown in Figure 68.

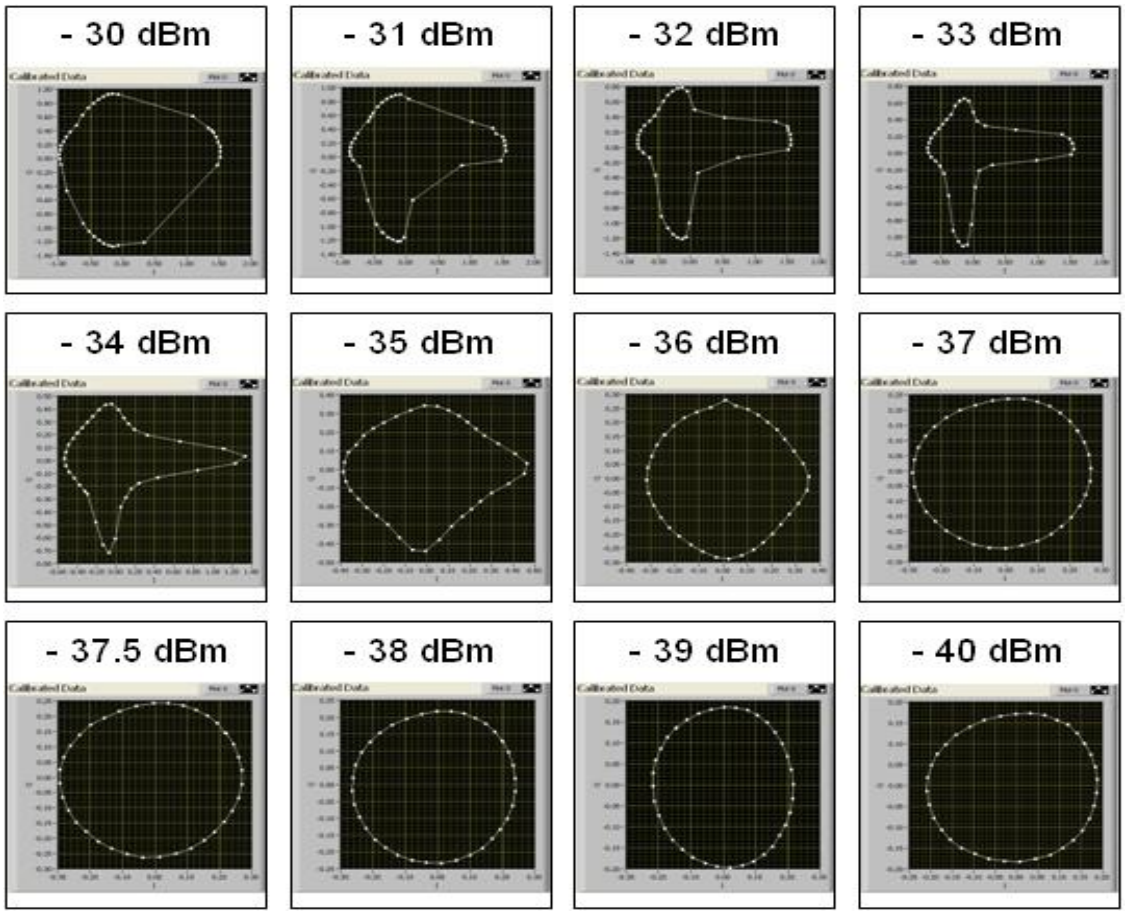

Figure 67. I and Q Circles from -30 dBm to -40 dBm.

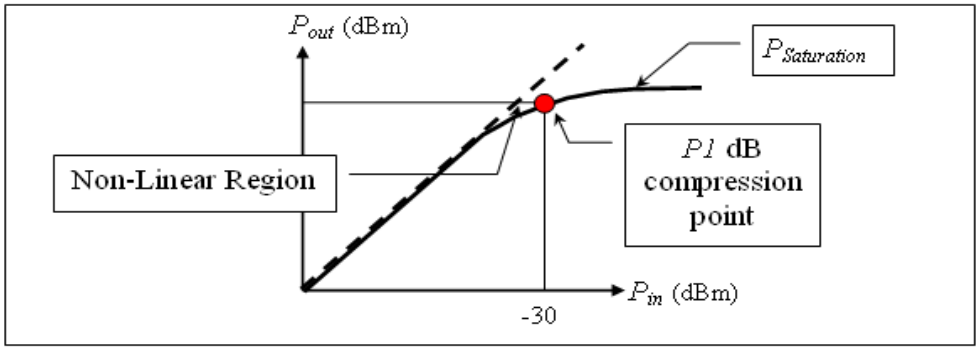

Figure 68. Non Linear Region near P1 dB.

The smallest delta is recorded at -37.5 dBm, which formed the most ideal I and Q circle. The power level after -37 dBm is observed to be decreasing slowly with minimum delta. Thus, it can be concluded that the optimum setting for RFIN to the demodulator board is about -37.5 dBm.

E. EFFECTS OF THE SAMPLING SIZE

The effects of different sampling sizes (or record lengths) were examined at 1,000,000, 10,000 and 1,000 samples per phase step. The results recorded are as shown in Figure 69.

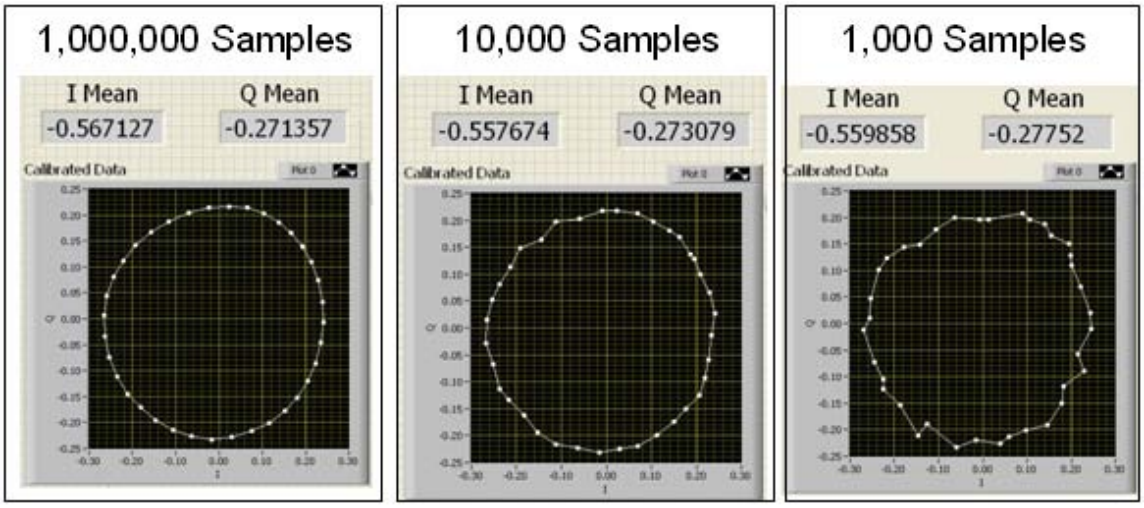

Figure 69. Calibration Results at 1,000,000, 10,000 and 1,000 Sample Size.

By comparing the three I and Q circles, it can be observed that I and Q circle at 1,000 sample size has the worst deformed shape of a circle. But as the sampling size increases, the I and Q circle at 1,000,000 sampling size produced the best results. More sampling reduces the effects of noise, thus 1,000,000 is recommended as the default sampling size for future calibration. However, it was observed that the shape of the circle in terms of deformity does not greatly affect the calibrated I and Q offset values, as the difference between the three sample sizes are small.

F. EFFECTS OF PHASE SHIFT STEP SIZE

The effects of changing the phase shift step size were examined by using step sizes of 10^0 and 5^0. The results recorded are as shown in Figure 70.

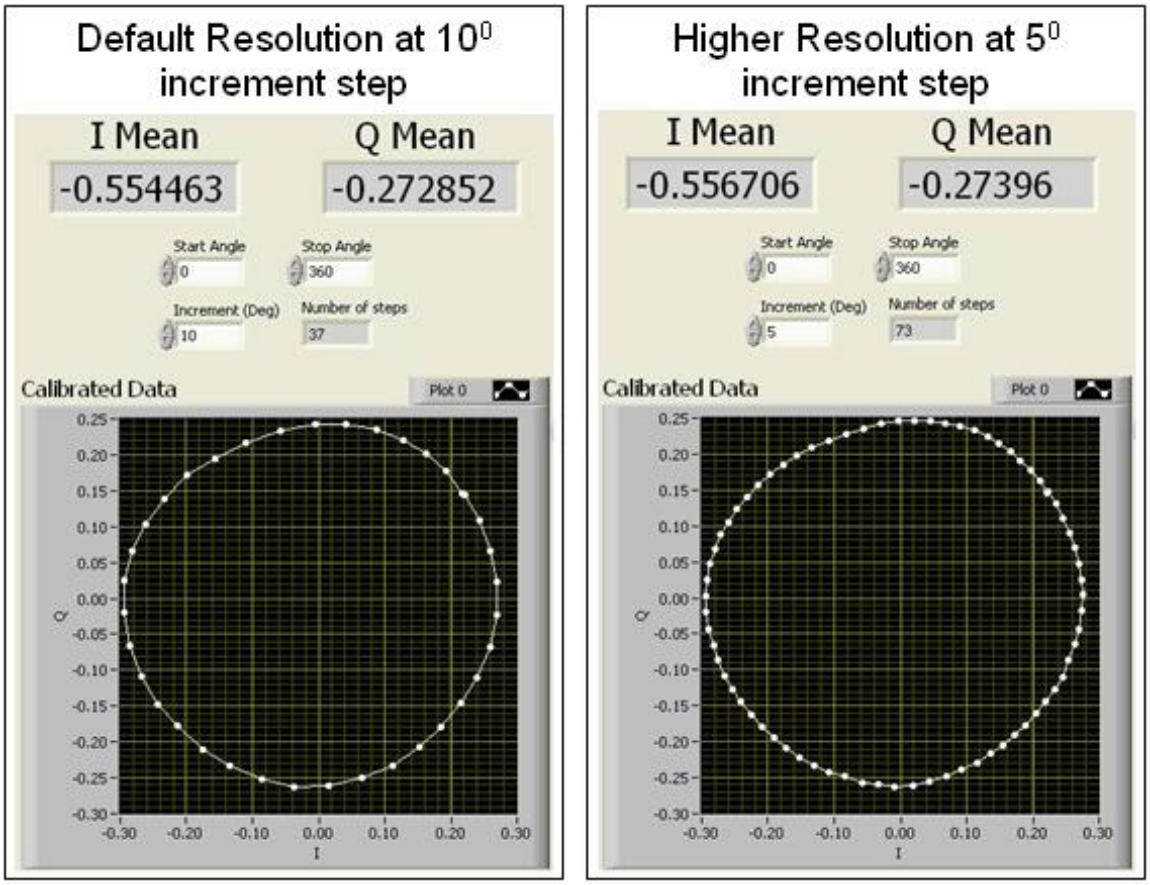

Figure 70. I and Q Circle at 10^0 and 5^0 Increment Step.

The IQ circle formed using 5^0 increment step has more phase points, increasing from default 37 points to 73 points. However, the I and Q mean values are almost the same as the default 10^0 increment step (changes at the third decimal places). Thus, it is recommended to set the default at 10^0 due to shorter calibration time.

G. EFFECTS OF I AND Q AMPLITUDE

The effects of I and Q amplitude sent to the modulator board for phase shifting were examined by using amplitudes of 2 V and 1.2 V. Measurements were recorded and are shown in Table 1.

IQ Amplitude at 2 V		
Result #	I	Q
1	-0.554897	-0.279421
2	-0.55421	-0.278733
3	-0.554375	-0.278534
4	-0.552272	-0.279499
5	-0.551437	-0.278824
Average	-0.5534382	-0.2790022

IQ Amplitude at 1.2 V		
Result #	I	Q
1	-0.550655	-0.280221
2	-0.549972	-0.279734
3	-0.550387	-0.279651
4	-0.549885	-0.280111
5	-0.550285	-0.279867
Average	-0.5502368	-0.2799168

Table 8. Measurements of I and Q at Amplitude 2 V and 1.2 V.

The average I and Q values calculated for both amplitudes were close, thus amplitude does not affect the calibrated I and Q values as the difference between them is marginal (the third decimal place). The only observed difference between the two results was the size of the circle as shown in Figure 71. I and Q amplitude at 2 V setting produced a bigger circle than at 1.2 V setting. This is due to the I and Q components' relationship to the amplitude given by Equation (2.6). Thus it recommended to set the default I and Q amplitude to 2 V according to specification of AD8346 modulator card [19].

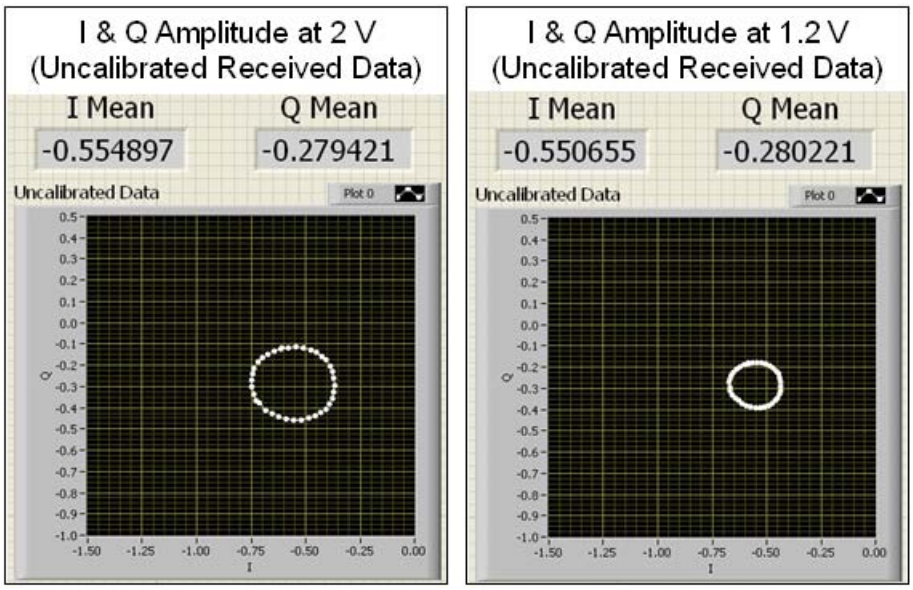

Figure 71. I and Q Uncalibrated Circle at Amplitude 2 V and 1.2 V.

H. SUMMARY

In this chapter, the calibration procedures and the different validation tests carried out were described. The calibration procedures elaborate the steps needed for a calibration session. The validation tests examined the characteristics of the calibration station in detail and concluded by recommending default parameter settings. In the next chapter, concluding remarks and suggestions for future work will be discussed.

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V. CONCLUSIONS AND RECOMMENDATIONS

This chapter covers the conclusions of the calibration results based on the validation tests carried out to assess the robustness and accuracy of the new calibration station. Last but not least, some recommendations for future work to further improve hardware and software are presented.

A. SUMMARY AND CONCLUSIONS

The focus of this thesis was to improve the existing manual calibration station for ease of use, shorter calibration time, repeatability, accuracy and versatility for future modifications and breadboarding. Several validation tests were conducted to verify the hardware and software of this new automated calibration station. The test conducted to validate the automated station against the manual calibration was positive as the calibrated I and Q offset values for both calibration stations were almost the same with only less than 3.15% difference. It is believed that the automated test is actually more accurate, because the mechanical phase shifter introduced error due to wear and tear, dirt, etc.

The automated calibration process was also more time efficient, taking only 1/10 of the manual calibration duration and helping the user avoid the chore of manually turning the phase shifters. With the verified accuracy and improved efficiency, more tests can be conducted on each board in order to calculate their average. Thus, we can extract more accurate final I and Q offset values as compared to the existing manual calibration.

Tests were carried out to characterize the performance of the new automated calibration station. Important conclusions from such tests help to mold the characteristics of the automated calibration station. By studying the effects of using different PXI-5112 digitizer cards, it can be concluded that using different digitizer card indeed gives some differences in the final calculated I and Q offset values. For some applications, it might be necessary to use the same digitizer for both calibration and in the system hardware.

Important parameters and their default values for calibration were also defined through tests. They include the optimized RFIN power level setting to the demodulator card, the most efficient I and Q increment steps for phase shifting without suffering degradation in performance, and the optimized amplitude of the I and Q components for phase shifting. After examining the effects of different sampling sizes (record lengths), it can be observed that higher sampling size will only give a smoother circle without distortion but may not necessarily improve the accuracy of the offset results significantly.

Six AD8347 demodulator cards used in the tracking array developed for UAV Tracking Array Development and Testing [30] were calibrated using the station described in this thesis. Two sets of phase calculations for the tracking array were executed, one using calibrated I and Q offset values and the other without the offsets. With calibrated I and Q offset values, the tracking array is able to retrieve the phase information of the incoming waveform thereby allowing the array to successfully track the signal AOA. Thus, the test indicates a successful implementation of the AD8347 demodulator card using this new automated calibration station.

B. RECOMMENDATION FOR FUTURE WORK

Further efforts can be explored to expand its application and the possibility of integrating it into other system architectures as a built-in calibration and test or to operate as a stand-alone system.

1) Integrating calibration features into systems

The current tracking array and distributed digital array radar (DDAR) [3] systems have no built-in calibration or test capability. Demodulator boards are calibrated using the calibration station prior to installation in the system. The calibrated I and Q values are then imported separately into the tracking array program. It also indirectly creates the inconvenience of demodulator card removal in the event of re-calibration is required. Ultimately, the goal is to integrate the automated calibration function into the tracking array and DDAR systems.

2) Self-test or built-in test (BIT) for the tracking array system

The calibration station can also be integrated into a system for self-test or built-in test (BIT) features, besides serving the primary role of calibrating the demodulator board. The tracking array system currently has no means of detecting a faulty demodulator card. Thus, the calibration station can utilize its phase-shifting features with its AD8346 modulator card for this purpose. This capability allows the system to reconfigure or adapt to changes that occurs in the system (e.g., failure).

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